Electronics and DAQ

Graduate Instrumentation and Detector School (GRIDS2018)

June 10 – 21, 2019

TRIUMF DAQ group

Pierre-André Amaudruz

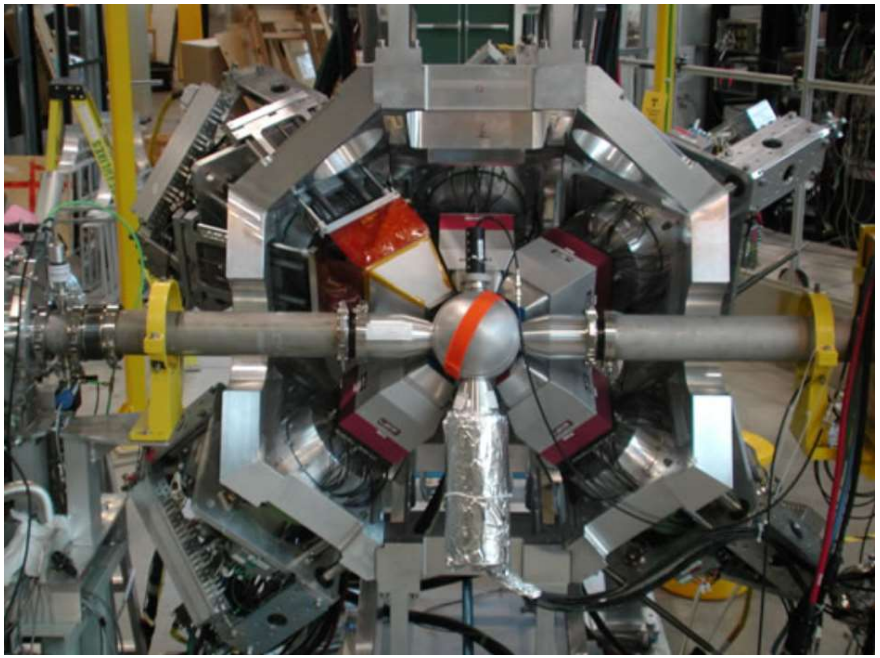
30th Anniversary of the World Wide Web

"***Suppose all the information stored on computers everywhere were linked. Suppose I could program my computer to create a space in which everything could be linked to everything.***"

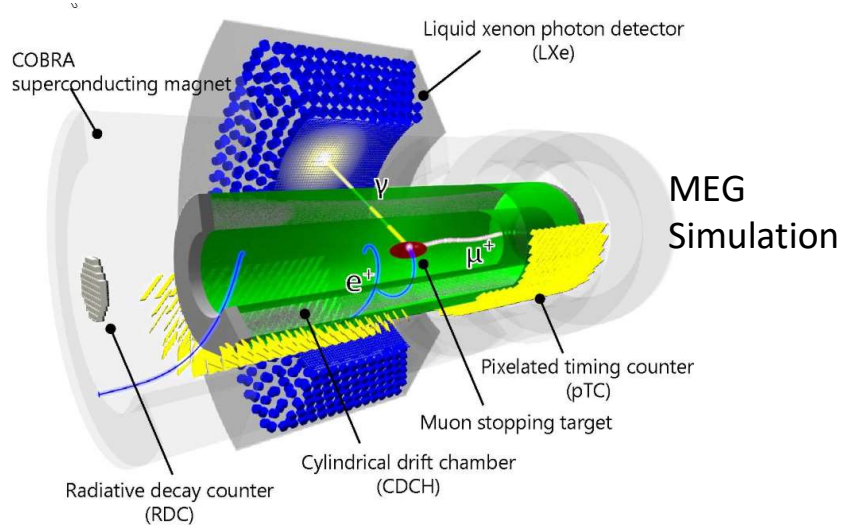
Tim Berners-Lee, inventor of the World Wide Web

Where does the Data Acquisition fit in the big scheme?

- A link between the experimental hardware and the data analysis
- Need attention during the experiment concept phase
- Provides the early tools for validation of the experiment.

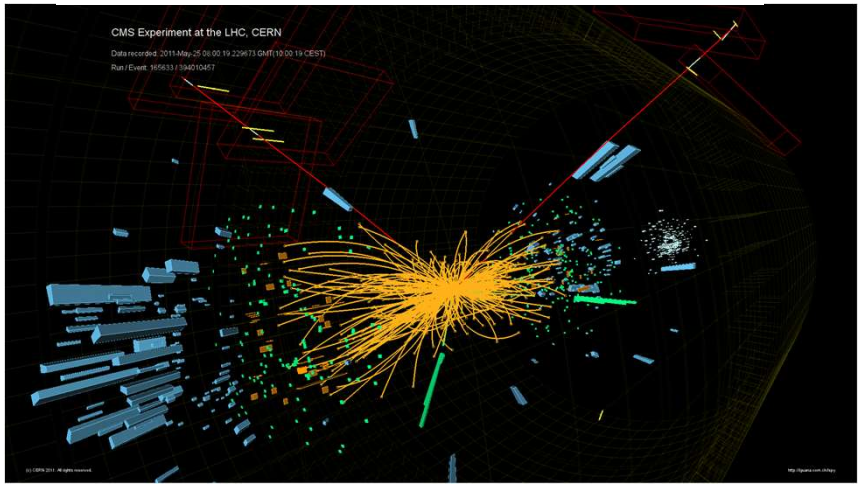


Tigress Experiment



MEG Simulation

- Position {x,y,z}, {r,θ,z} → direction
- Time {relative, absolute} → speed, position
- Energy deposit → PID
- B-field, position → Charge, momentum

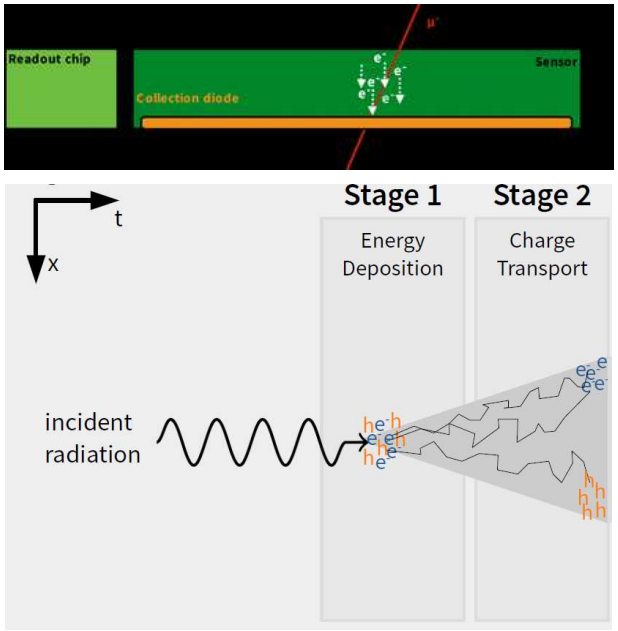


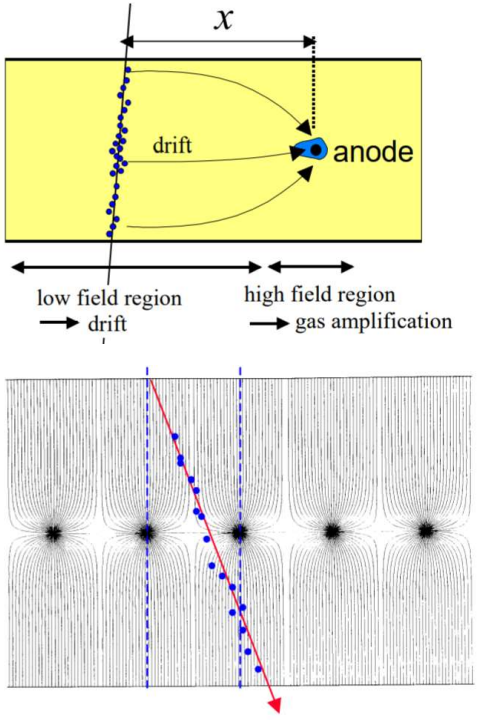
CMS Monitoring

Detectors

- Converts the phenomenon under study to physical perturbation of its surrounding that can be measured/ recorder – in a different space and time frame –
- ***Whatever the perturbation method is, the expected information to record is an electrical signal***
  – Photo detector & Gas/Drift chambers in general –

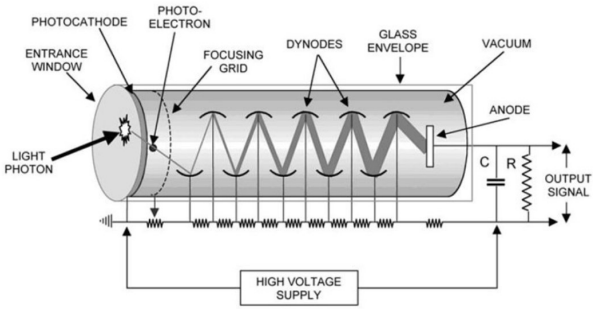
SIPM





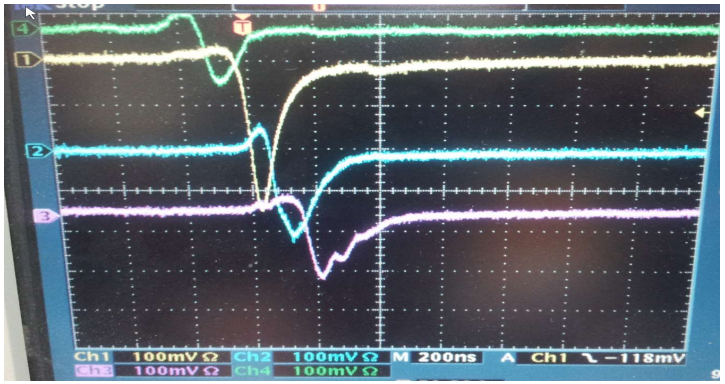
Charge deposition in a localized volume

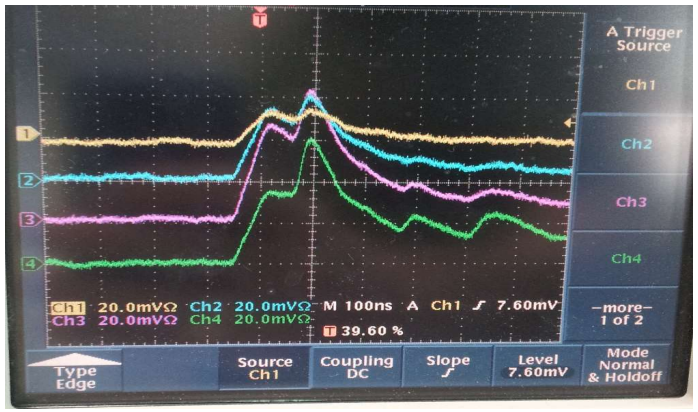
- Wire chamber: position(wire), (time)
- Drift chamber: position(time)
- Scintillator: time, energy, (position)
- Silicon based: time, position, energy
- Other type but similar information



Electronics

- Condition the detector signals to a more suitable electrical signal for transport, digitization range [amplitude, time] – Pre-Amplifiers, Shaper/Filter, Discriminator –



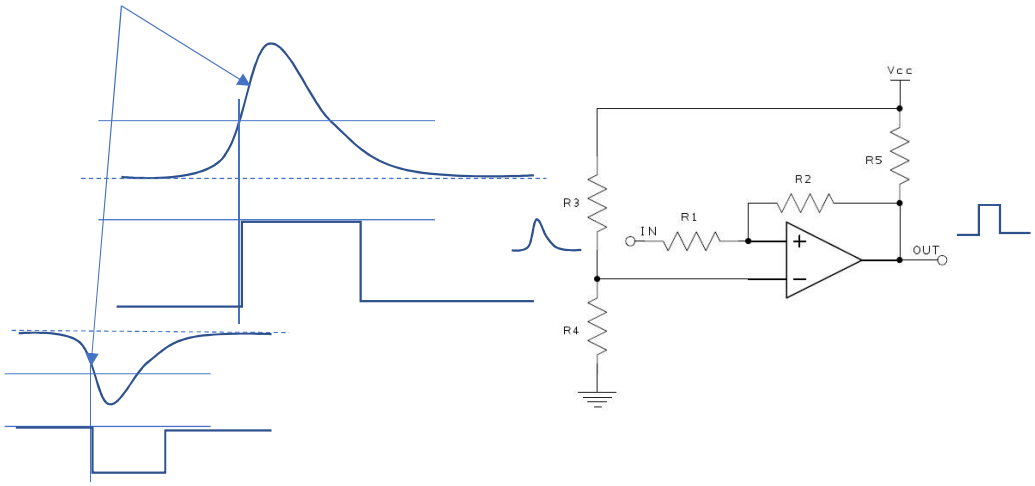


- Signal Shape
- Is it noise?
- Noise impact on Amplitude and Time
- Discrimination of the signal
- Digitization of the signal

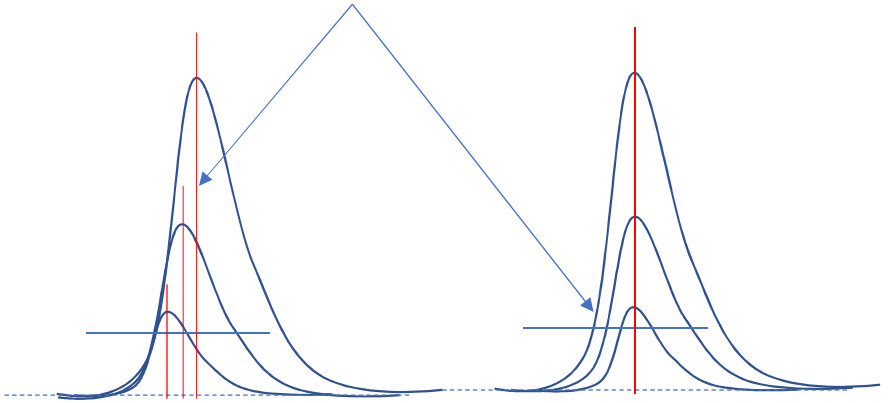
Electronics – Discrimination

- Produce a new binary signal out of an Analog signal for presence detection or timing purpose
  - Leading Edge detection [LE]
  - Constant Fraction Discriminator [CDF]

Leading Edge



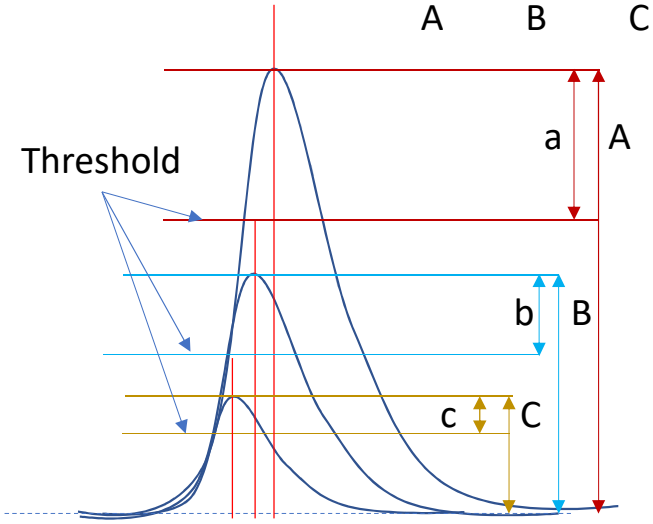
Time Walk

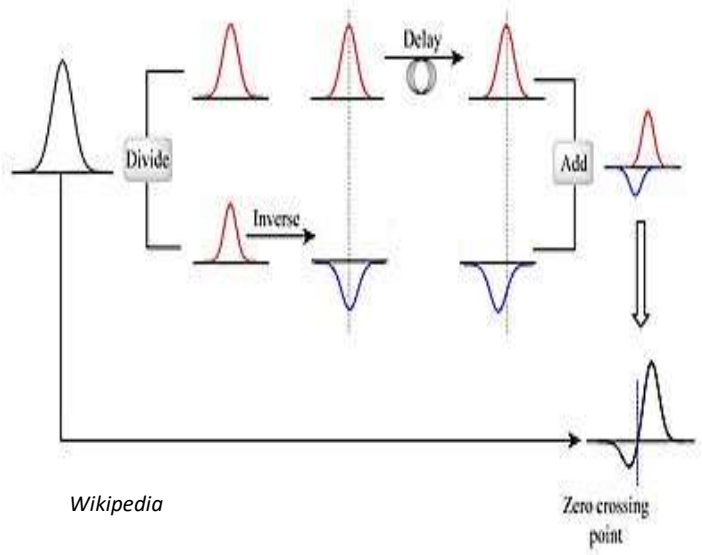


Electronics – Discrimination

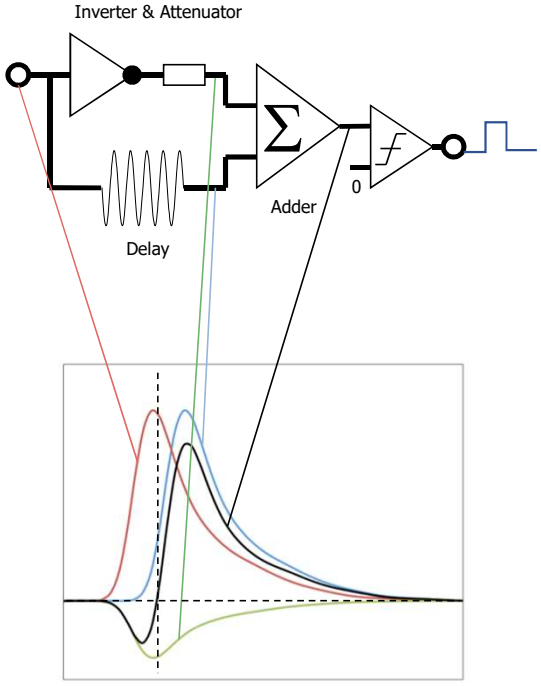
- Produce a new binary signal out of an Analog signal for presence detection or timing purpose
  - Leading Edge detection [LE]
  - Constant Fraction Discriminator [CFD] – dynamic threshold setting based on the signal amplitude

$$\frac{a}{A} = \frac{b}{B} = \frac{c}{C} = \text{Constant}$$





Wikipedia



Stefan Ritt

Electronics – Digital signal levels

- Multiple type of digital signals available, evolved based on:
  - Logic Family
  - Need for Speed
  - Reduce current consumption
  - Improve immunity to interference

TTL (CMOS-TTL) VOL= [0.0:0.4]V , VOH= [2.4:5]V

NIM VOL=0V, VOH=-0.8V, IOH=[-14:-18]mA, IOL=[-1:+1]mA @50Ω

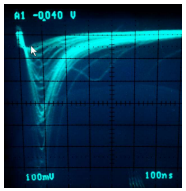
BNC, LEMO00, SMA/B, MCX connectors
Coaxial type

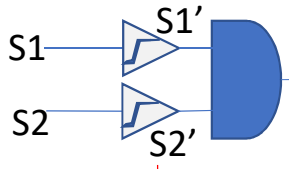
Differential ECL (pECL) VOL=[-1.95:-1.6]V , VOH=[-1.0:-0.75]V

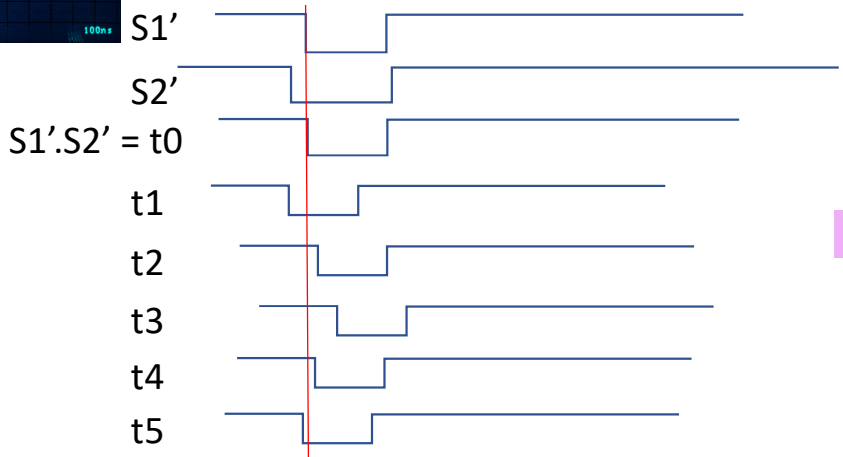
Differential LVPECL VOH=2.4V, VCM=2.0V, VOL=1.6V (800mV swing)

Differential LVDS VOH=1.4V, VCM=1.2V, VOL=1V (400mV swing)

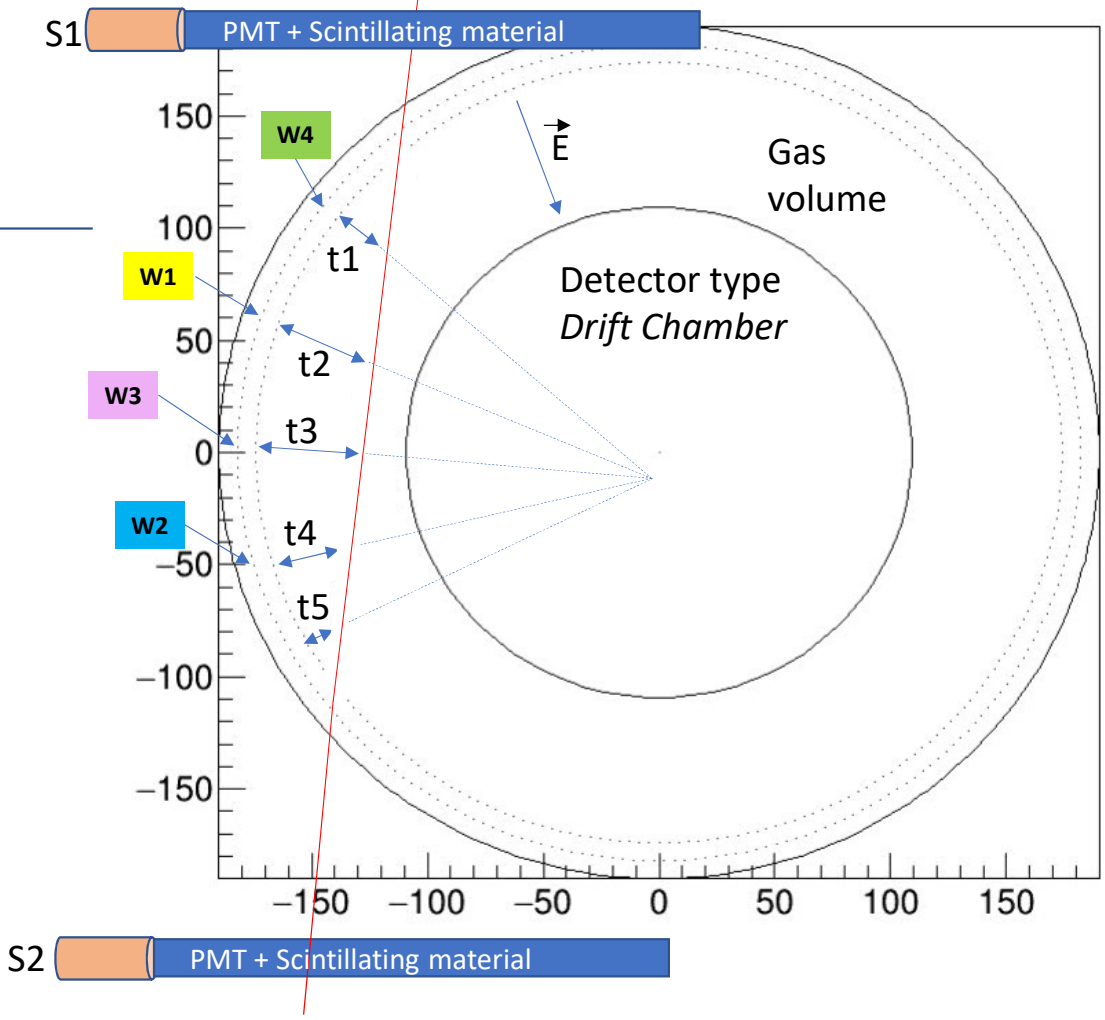
Pair of pins per signal
Twisted pair cable




S1
S1'
S2
S2'
t0

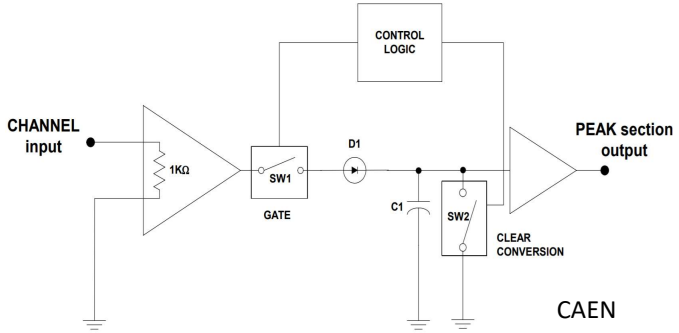

S1'
S2'
S1'.S2' = t0
t1
t2
t3
t4
t5

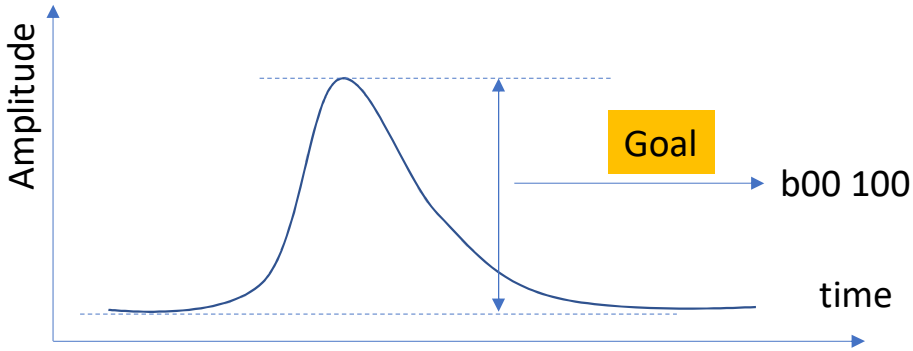

Detectors signals Wx

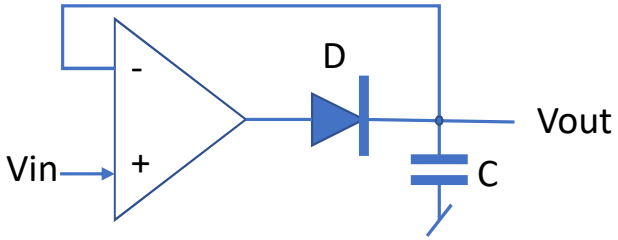

S1
PMT + Scintillating material
W4
W1
W3
W2
E
Gas volume
Detector type
Drift Chamber
t1
t2
t3
t4
t5
150
100
50
0
−50
−100
−150
−150 −100 −50 0 50 100 150
S2
PMT + Scintillating material

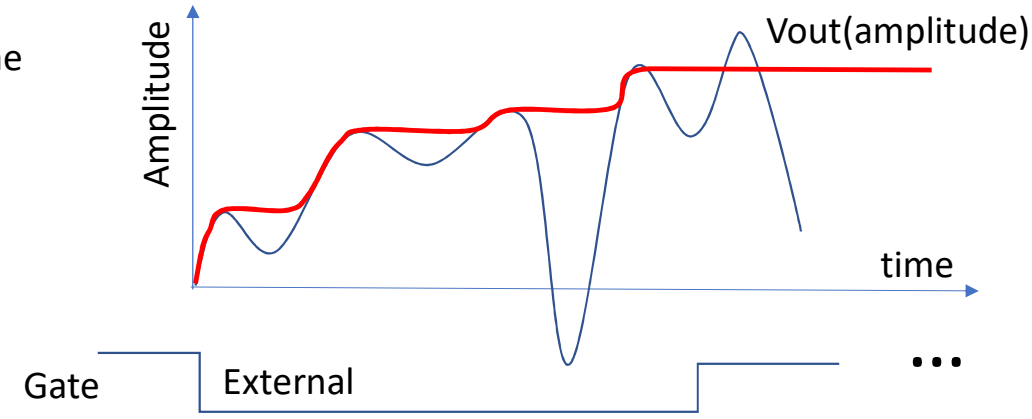
Electronics – Amplitude Digitization…

- Convert one of the Analog signal feature to its binary representation (digital form)
  - Discrimination (one bit)
  - Amplitude to Digital Converter [Peak sensing ADC]
  - Charge to Digital Converter [QDC, or ADC (A to D)]
  - Time to Digital Converter [TDC]



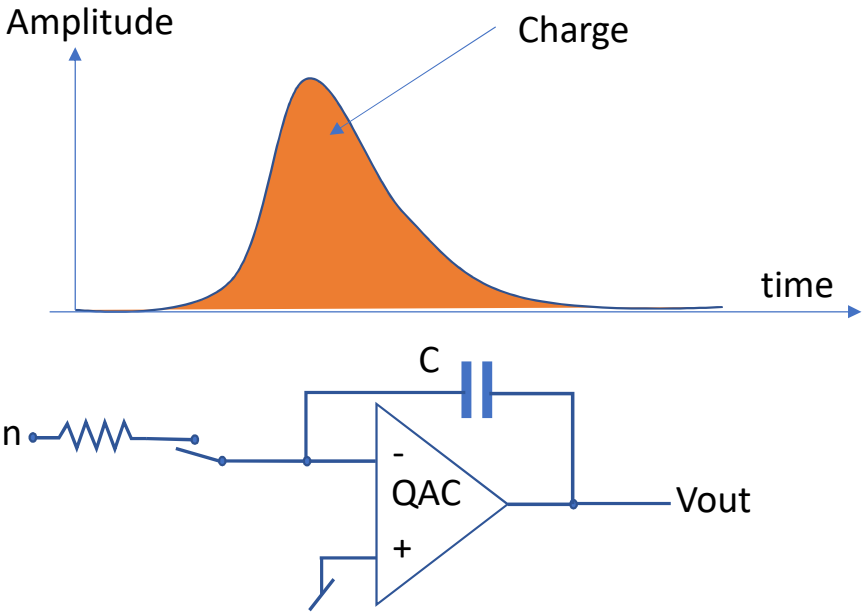


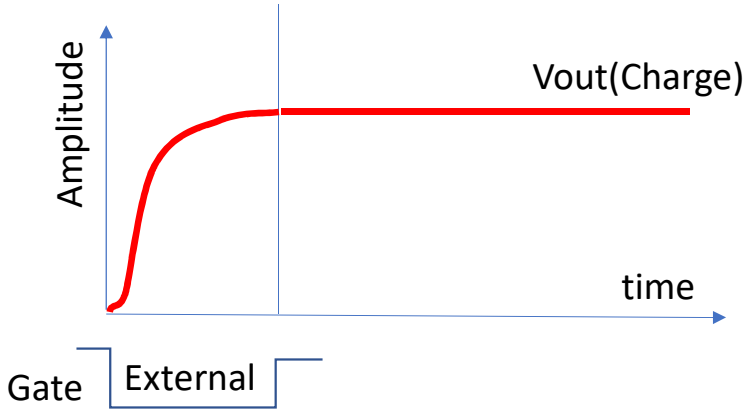




Electronics – Charge Digitization…

- Convert one of the Analog signal feature to its binary representation
  - Discrimination (one bit)
  - Amplitude to Digital Converter [Peak sensing ADC]
  - Charge to Digital Converter [QDC, or ADC (A to D)]
  - Time to Digital Converter [TDC]

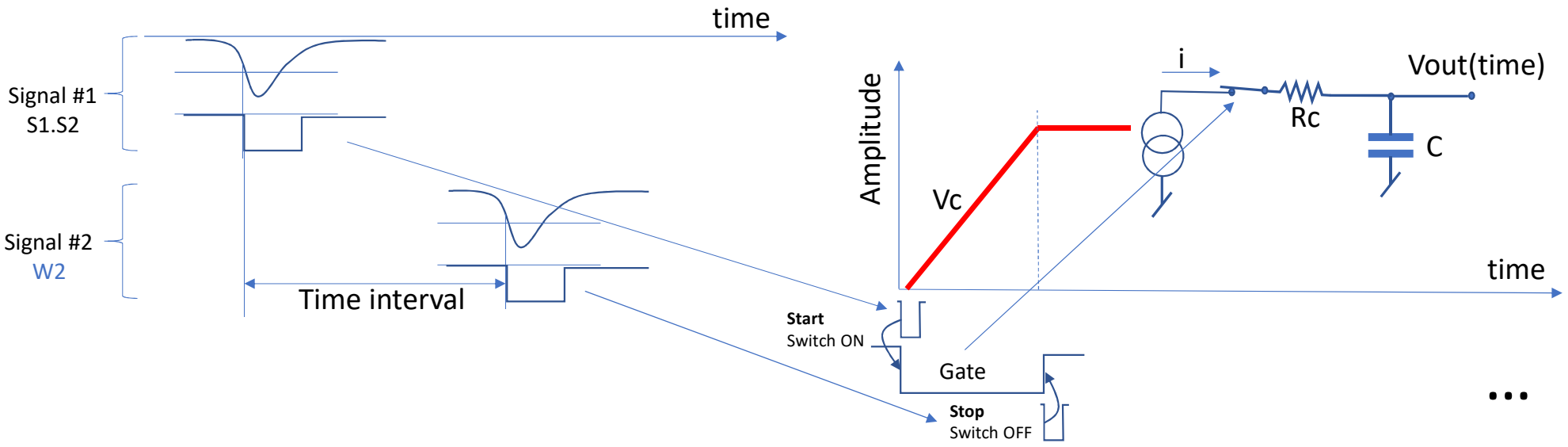




…

Electronics – Time Digitization…

- Convert one of the Analog signal feature to its binary representation
  - Discrimination (one bit)
  - Amplitude to Digital Converter [Peak sensing ADC]
  - Charge to Digital Converter [QDC, or ADC (A to D)]
  - Time to Digital Converter [TDC]

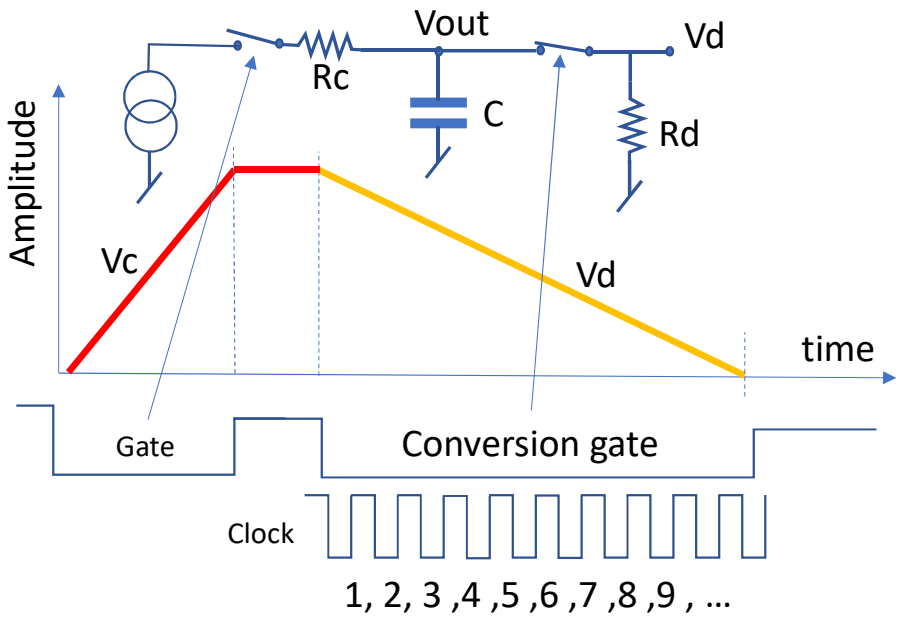


Electronics – Analog to Digital Converter

- ADC translate the analog signal amplitude to its digital representation
- How fast can I convert a voltage level to its binary representation?
- Different methods
  - Wilkinson ADC, dual-slope, etc.

  Time of discharge proportional to Vout
  Time measured in number clock period

  Limited by the clock rate for Hi-Resolution
  Conversion time dependent on the amplitude range
  Excellent linearity
  Tradeoff : Speed versus Precision

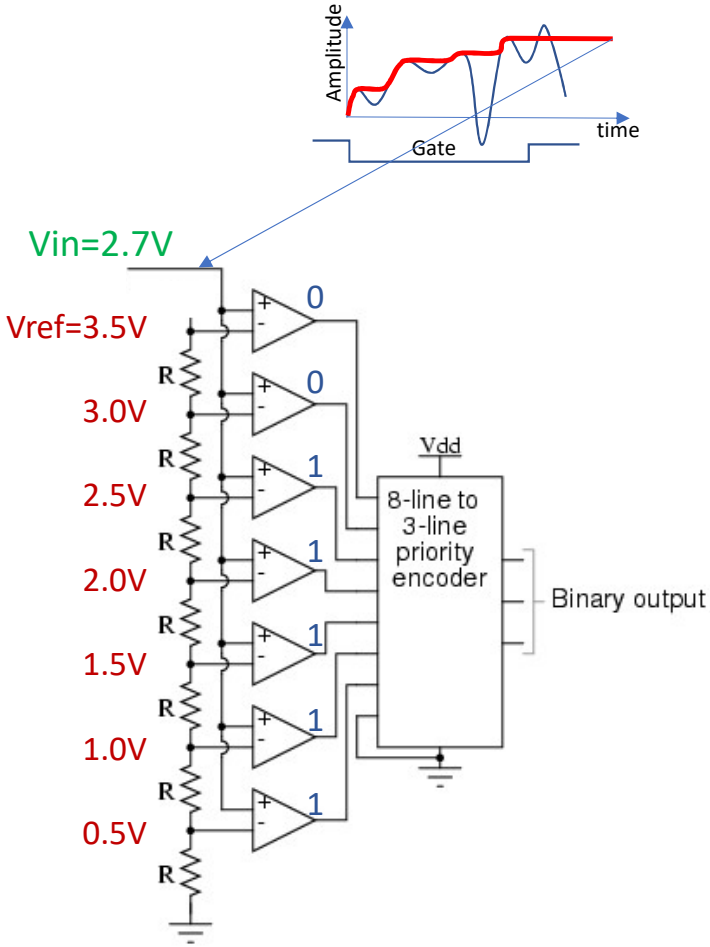


Electronics – AD Converter

- ADC translate the analog signal to its digital representation

- Different methods
  - Wilkinson ADC, dual-slope, etc
  - 1, 2, n-bit Flash ADC

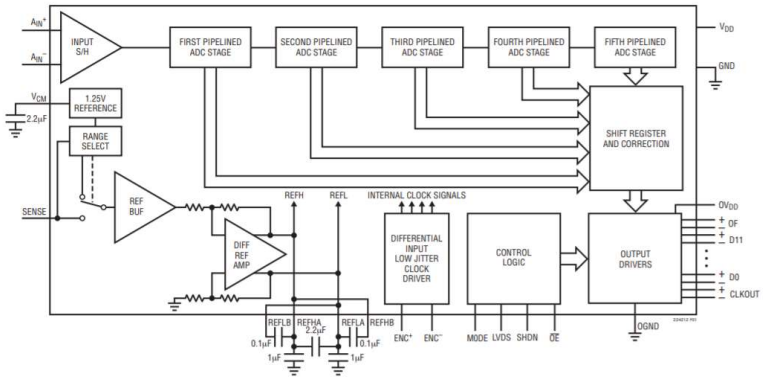
  Requires 2^n Comparators for n output bits!
  Requires calibrated "resistor chain"
  Fastest conversion time – for small number of bits –
    - ➢ Possible to keep converting the input signal

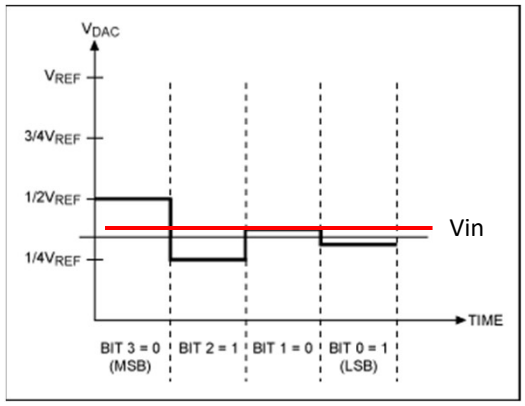


Electronics – AD Converter

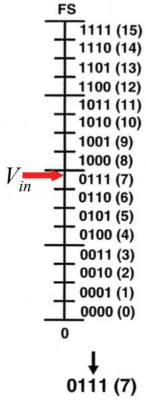
- ADC translate the analog signal to its digital representation
- Different methods
  - Wilkinson ADC, dual-slope, etc
  - 1, 2, n-bit Flash ADC
  - Successive Approximation (SAR), Pipeline, Combination of SAR and Flash
  - Sigma-Delta ADC (Vin as Vref, oversampling/decimation)

LTC2242 12bits@250Msps

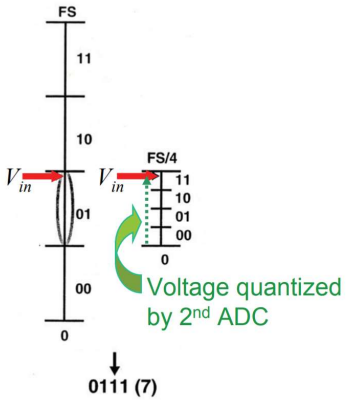


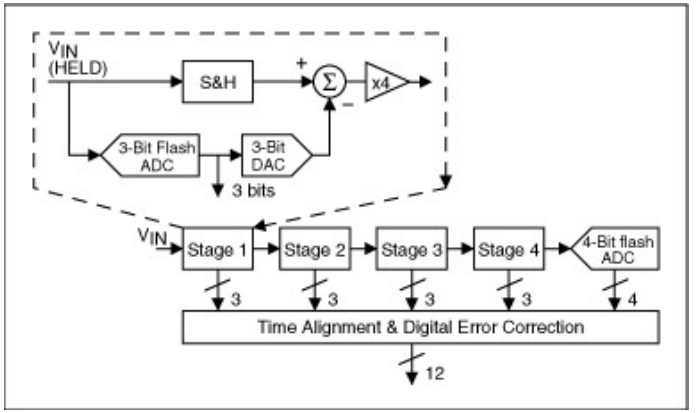


4-bit Straight Flash ADC



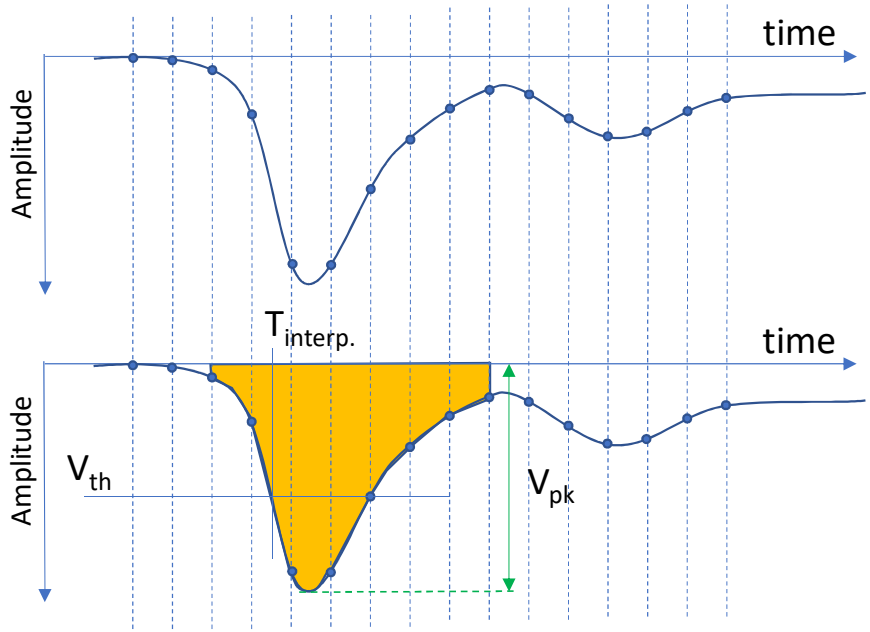
Ideal 2-step Flash ADC





Electronics – WaveForm Digitization

- Digitize the signal waveform
  - Extract signal features within the digital world (DSP)
  - Expected waveform based on the collected data (Q, V_{pk}, Time)

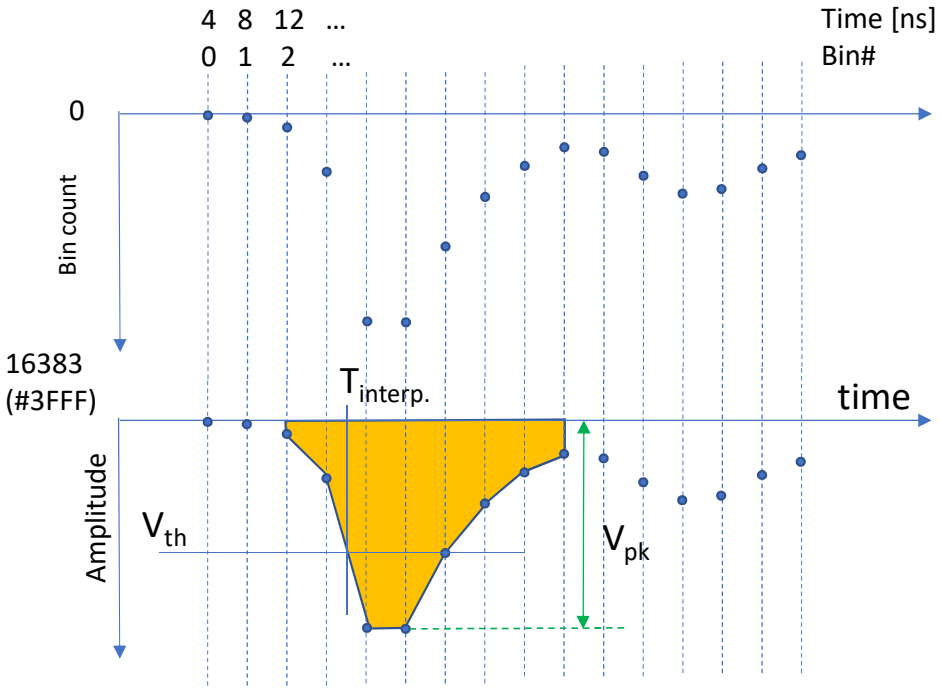


Type of ADC	Resolution (max. bits)	Conversion rate (max.)
Dual slope	12-20	100 samples/s
Successive approximation	8-18	10 Msamples/s
Flash	4-12	10 Gsamples/s
Pipeline	8-16	1 Gsample/s
Delta-sigma	8-32	1 Msample/s

Electronicdesign

Electronics – WaveForm Digitization

- Digitize the signal waveform [WFD]
  - Collect amplitude values at fix time interval
  - Within the digital world (DSP), signal features can be extracted

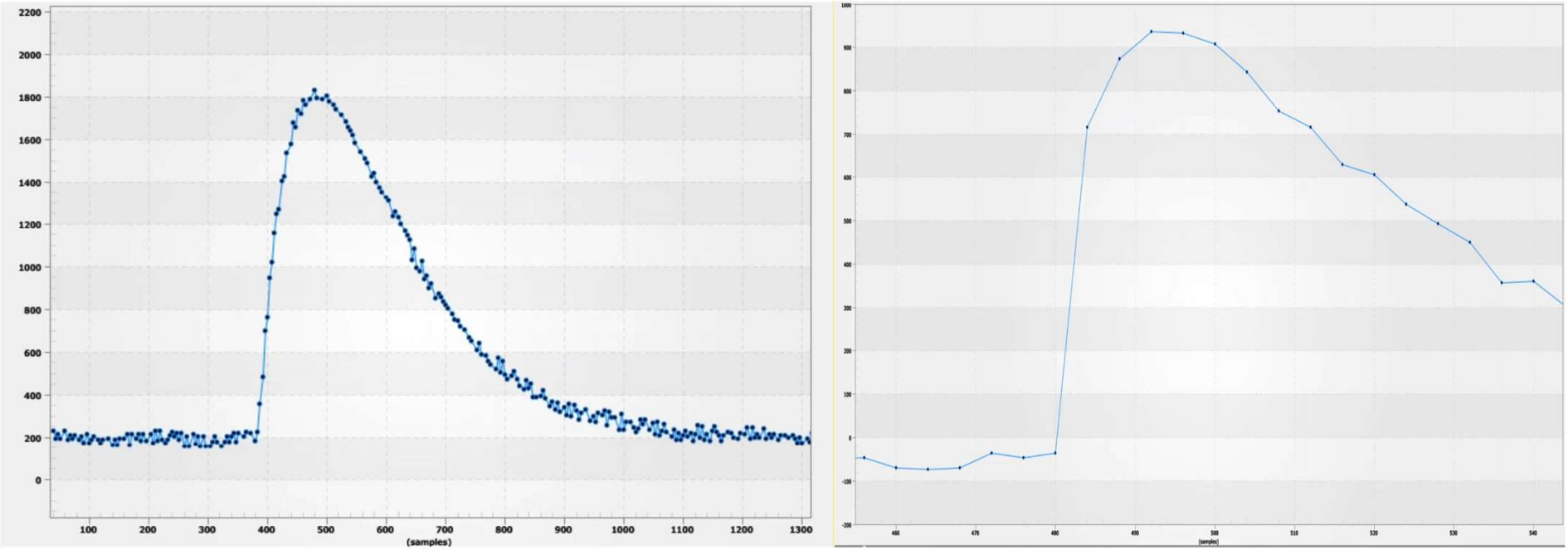


CAEN V1725 : 14-bit@250Msps
Time bin = 4ns

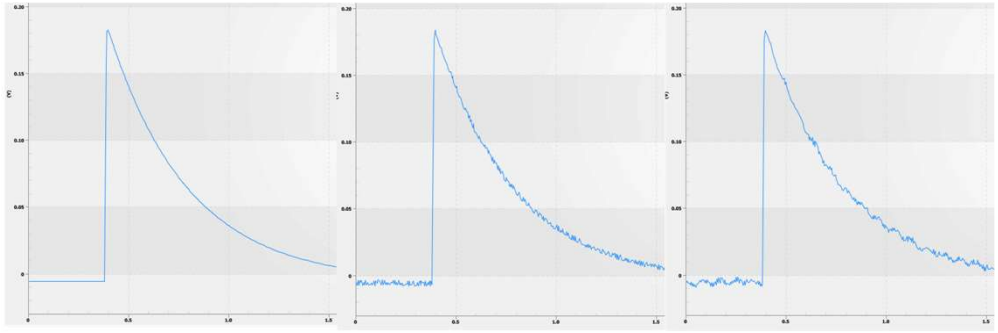
…
1-> 0xa0007d14 0x000002ff 0xff00987f 0x13a291b7 0x3c1807d1 0x3c183c1c 0x3c1a3c19 0x3c1b3c18
9-> 0x3c1c3c16 0x3c193c12 0x3c1a3c19 0x3c163c18 0x3c183c1a 0x3c163c17 0x3c1f3c17 0x3c193c18
17-> 0x3c183c19 0x3c183c1a 0x3c193c1b 0x3c173c19 0x3c193c14 0x3c1b3c18 0x3c183c16 0x3c183c18
25-> 0x3c173c19 0x3c1a3c19 0x3c183c19 0x3c183c12 0x3c183c1a 0x3c193c19 0x3c1c3c14 0x3c173c19
33-> 0x3c193c14 0x3c193c16 0x3c153c1a 0x3c1b3c15 0x3c183c16 0x3c163c19 0x3c193c17 0x3c1c3c19
41-> 0x3c1a3c18 0x3c193c17 0x3c193c15 0x3c173c1b 0x3c183c17 0x3c163c18 0x3c173c15 0x3c163c1a
49-> 0x3c1c3c14 0x3c173c1c 0x3c193c16 0x3c183c19 0x3c193c16 0x3c173c1a 0x3c173c17 0x3c1b3c18
57-> 0x3c163c13 0x3c193c17 0x3c163c19 0x3c1d3c15 0x3c1b3c18 0x3c163c19 0x3c1b3c1a 0x3c153c1c
65-> 0x3c183c1b 0x3c1c3c16 0x3c193c17 0x3c193c18 0x3c183c1a 0x3c193c1a 0x3c173c18 0x3c173c1d
73-> 0x3c173c17 0x3c1b3c1b 0x3c173c17 0x3c163c19 0x3c183c18 0x3c1c3c17 0x3c1c3c17 0x3c173c1b
81-> 0x3c173c18 0x3c183c19 0x3c1a3c19 0x3c193c1b 0x3c193c1b 0x3c1b3c19 0x3c173c16 0x3c1b3c18
89-> 0x3c1b3c15 0x3c193c1b 0x3c173c1a 0x3c163c1a 0x3c173c19 0x3c153c19 0x3c153c15 0x3c1c3c1c
97-> 0x3c183c14 0x3c1a3c17 0x3c183c1b 0x3c183c1d 0x3c183c15 0x3c183c16 0x3c1a3c16 0x3c1b3c1b
105-> 0x3c163c1b 0x3c163c18 0x3c193c15 0x3c193c14 0x3c163c1c 0x3c153c17 0x3c193c18 0x3c173c16
…

Electronics – Signal, noise

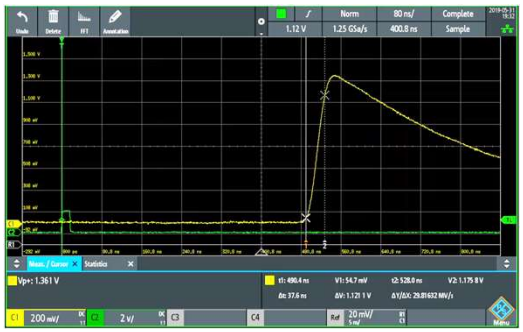
- How is the input signal?
- Need to condition the signal to match the digitizer (environment, cost)



Electronics – Shaping/Filter



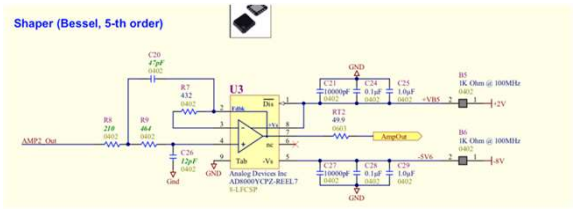
T_r=5ns, **τ**=500ns + random noise + 1/f noise (pink noise)



\+ Analog 7th order Bessel Filter

T_r=40ns (Noise: 1/5, Amplitude loss ~15%)

Filters: Butterworth, Bessel, Chebyshev



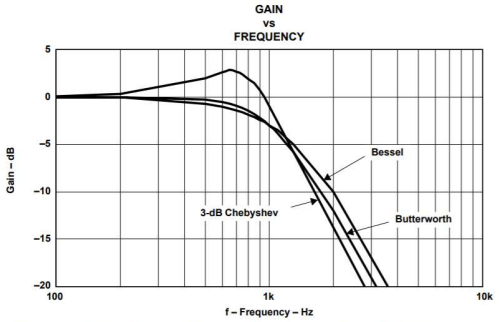
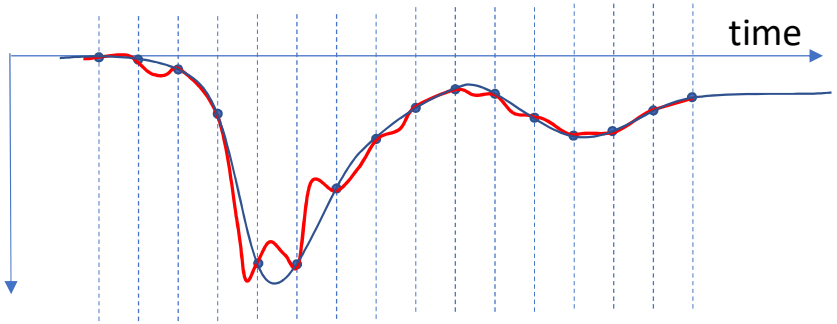


Figure 10. Second-Order Butterworth, Bessel, and 3-dB Chebyshev Filter Frequency Response

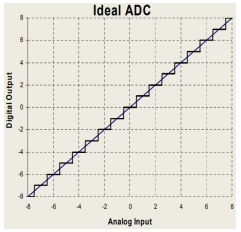
Electronics – WaveForm Digitization

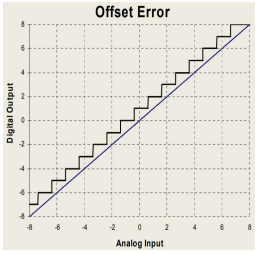
- Digitize the signal waveform
  - But this shape fits just the same!
    - Are you sampling the signal fast enough?
    - What is the bandwidth of the incoming signal?



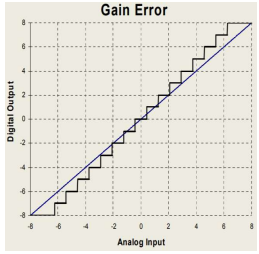
- Signal features can be extracted/improved in the digital world (DSP) only if the digital representation is faithful -> High sampling

Amplitude, Charge, timing measurement errors!

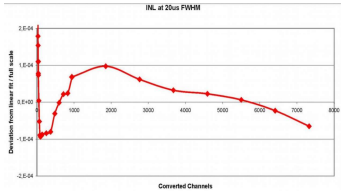




Can be corrected using a reference voltage

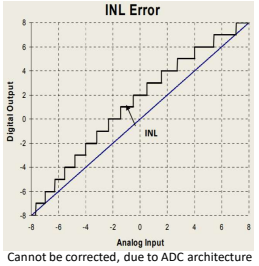


Slope issue, can be corrected using a second point reference voltage

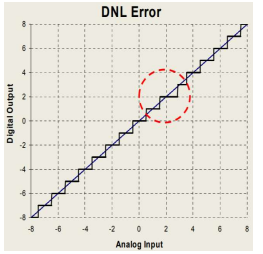


Example of INL (0.01%)

Mesytec



Cannot be corrected, due to ADC architecture

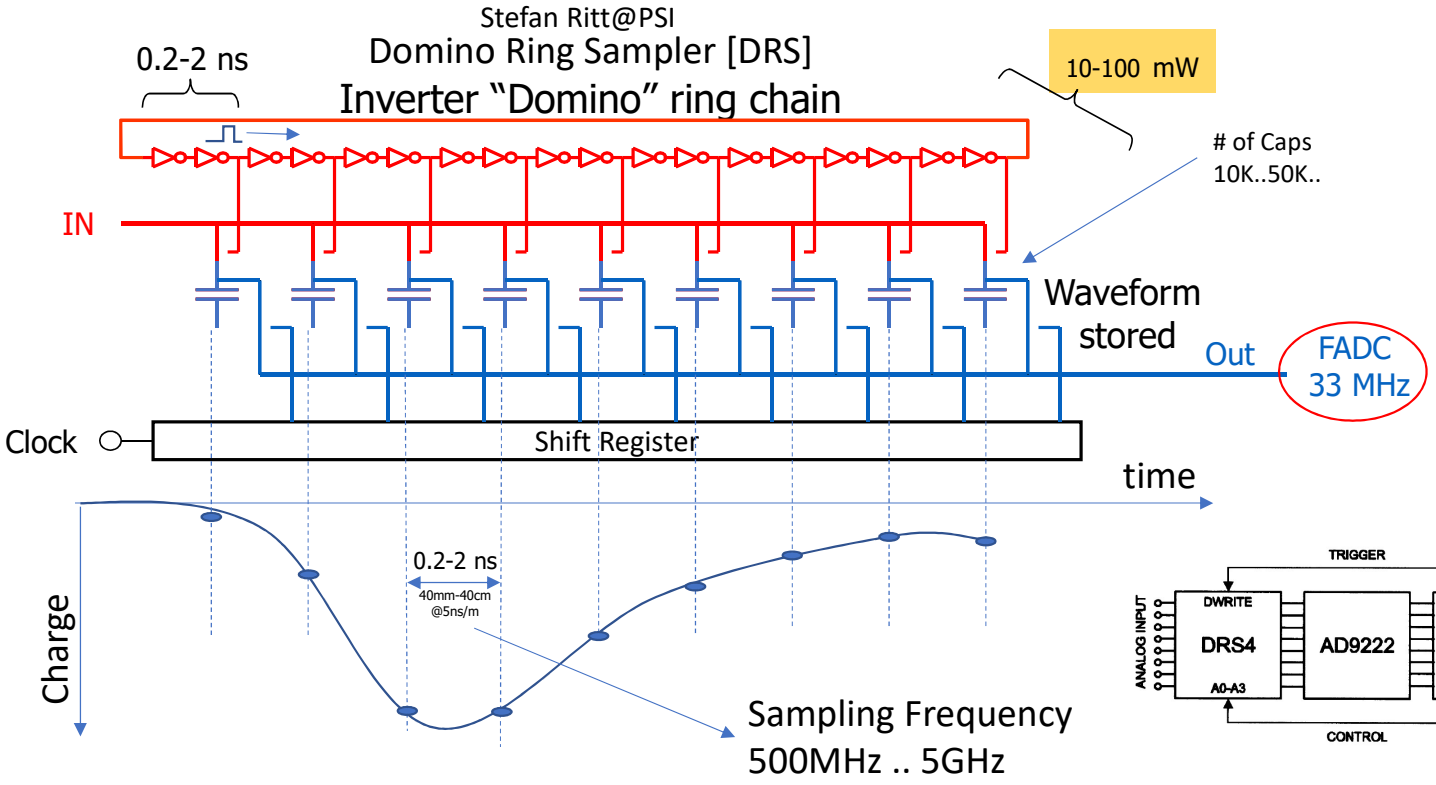


Cannot be corrected, due to ADC architecture

Cypress

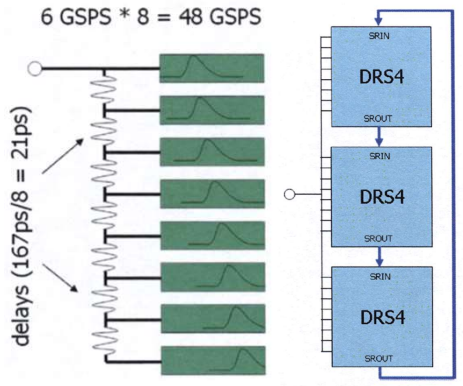
Electronics – [Application Specific Integrated Circuit (ASIC)] – WFD chip

- Yet another Waveform Digitizer architecture : **Switch Capacity Array [SCA],** an Ultra-Fast ADC ASIC



- ! individual cells are readout through a standard ADC at relatively low speed
- Need calibration in charge and time. All quantization errors apply to this architecture.
- Number of cell per chip is limited!

- But neat trick can be played!



Things to consider

- Pipeline architecture, Flash ADCs has "no conversion time" but has latency. Data come out of the ADC with an initial delay but with no deadtime in between samples.
  - But power hungry: ADS54J69 Dual-Channel, 16-Bit, 250..500Msps : $P_{dissipation}$ = 2..2.5W

- SCA do have a large dead time as each Analog cell needs to be converted to digital with standard ADC (20..50Msps)
  - Example: Acquisition of 72 ch. @ 512 cells/ch. Signal acquisition sampling frequency 100MHz (10ns)… Great! ☺
  - Readout speed 72 ch. * 512 cells @ 25MHz (40ns) => ~1.5ms => 680Hz max … what? But low power (10mW..100mW), high channel density (>8/chip)!

- Conversion issues
  - Know your signal dynamic range, match ADC specs?
  - Identify the possible source of error affecting the results
    - Signal noise, Digitization, quantization error, ...
  - Nyquist-Shannon theorem

  For acceptable signal fidelity $f_{sampling} > 2 * f_{signal}$
    - Sampling frequency (aliasing) - increase the sampling
    - Signal shaping (filters, bandwidth limitation circuit) - "slow down the input signal" -

Electronics – [Application Specific Integrated Circuit (ASIC)] – TDC chip

- Yet another way to digitize time interval

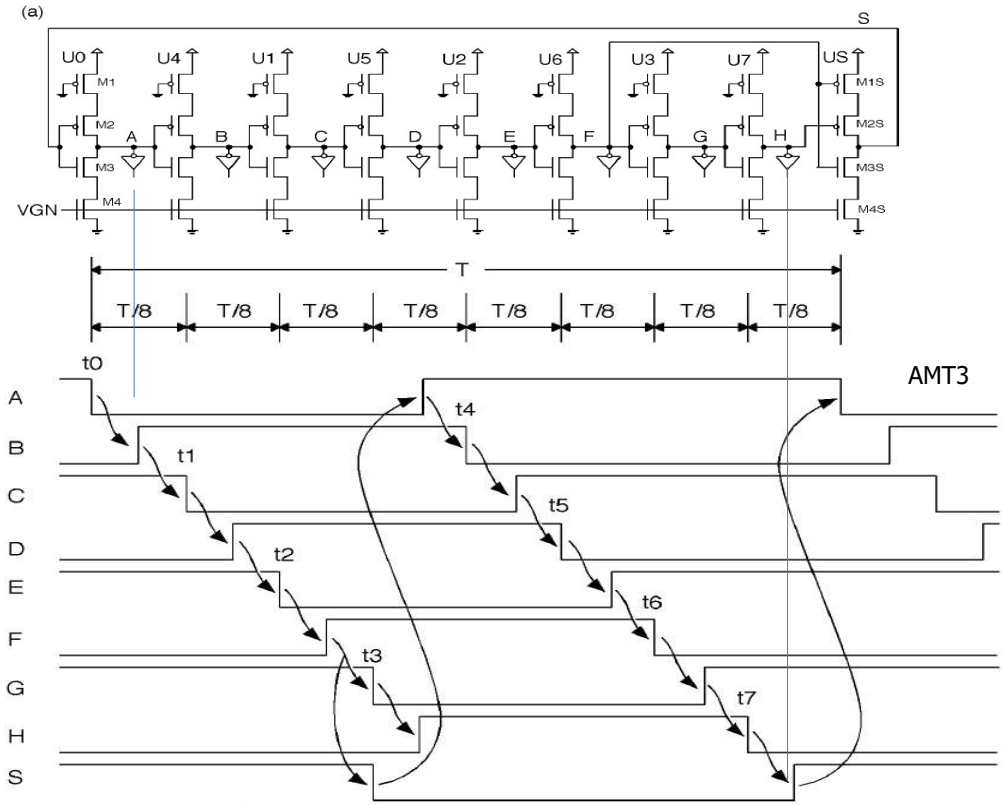


Fig. 2 (a) Asymmetric ring oscillator, (b) extracted timing signal.

Use gate delay to subdivide one clock period in even time interval, no dead time.

Example 1)
AMT-3 chip (ATLAS Muon TDC ver3)
24 Channels
Clock 40MHz x 2 = 80MHz -> 12.5ns
Number of tap 16 -> Time bin 781.25ps

Example 2)
HPTDC (High Performance TDC)
32 channels
Clock 40MHz x 8 = 320MHz -> 3.125ns
Time bin -> 25ps

Electronics – Field Programmable Gate Array (FPGA)

- ***ASIC*** *(**A**pplication **S**pecific **IC**) is for pure Analog circuitry or dedicated Digital Logic or Mixed electronics (Analog+Digital)*
  - *But in case of Digital Logic **only**, the Field Programmable Gate Array can be a better choice (cheaper).*

- **A**rray of electronic **G**ates that can be **P**rogrammed in the **F**ield (in-situ) for a specific function[s]
- Implement electronic logic circuitry in a "sea of gates"
  - Can be re-programmed at will
  - Has to have a "Simple" way to access the chip for changing its functionality…

- ***FPGA rules!***
  - Requires particular API to generate the downloadable device's code
  - Code is written in Verilog, VHL, VHDL, higher programming languages are available now…
  - Can instantiate processor[s] (soft core) or has additional System on Chip (SoC) already imbedded.
  - Can instantiate 64 channels TDC at 20ps time resolution! (trb.gsi.de)

  - FPGA is composed of
    - LEs or Lu's, ALMs (Logic Element/Unit, Adaptive Logic Module) - combination of AND, OR, FlipFlop -
    - Registers, Memory banks
    - Input / Output … see next slide!

Cyclone V SoC Features

[System on Chip]

	Product Line	Cyclone V SE SoCs[1]				Cyclone V SX SoCs[1]				Cyclone V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K) Logic Element	25	40	85	110	25	40	85	110	85	110
	ALMs Adaptive Logic Module	9,434	15,094	32,075	41,509	9,434	15,094	32,075	41,509	32,075	41,509
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (ARM Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual	Dual	Dual	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (MHz)	925	925	925	925	925	925	925	925	925	925
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	5	5	6	6	5	5	6	6	6	6
	PLLs (HPS)	3	3	3	3	3	3	3	3	3	3
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS									
	LVDS channels (receiver/transmitter)	37/32	37/32	72/72	72/72	37/32	37/32	72/72	72/72	72/72	72/72
	Transceiver count (3.125 Gbps)	–	–	–	–	6	6	9	9	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	9[4]	9[4]
	PCIe hardened IP blocks (Gen1)[5]	–	–	–	–	2	2	2	2	–	–
	PCIe hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	2	2
	GPIOs (FPGA)	145	145	288	288	145	145	288	288	288	288
	GPIOs (HPS)	181	181	181	181	181	181	181	181	181	181
	Hard memory controllers[6] (FPGA)	1	1	1	1	1	1	1	1	1	1
	Hard memory controllers[6] (HPS)	1	1	1	1	1	1	1	1	1	1
	Memory devices supported	DDR3, DDR2, LPDDR2									

Electronics – Bus standards

Where all this electronics plugs in?

NIM (1968): Nuclear Instrument Module

- Still in use for standard logic for workbench tests

CAMAC (1972): Computer Automated Measurement and Control, use TTL parallel bus

- Still in use in older system (Triumf Cyclotron Control).

VME (1981): Vesa Module Europcard

- Very much in use, as VME modules are still commercially available (parallel backplane bus).

~~FastBus (1984): To replace CAMAC with ECL parallel bus~~

- Dead

VXI (2004): **V**ME e**X**tensions for **I**nstrumentation

- Was an extension to fit a transition…

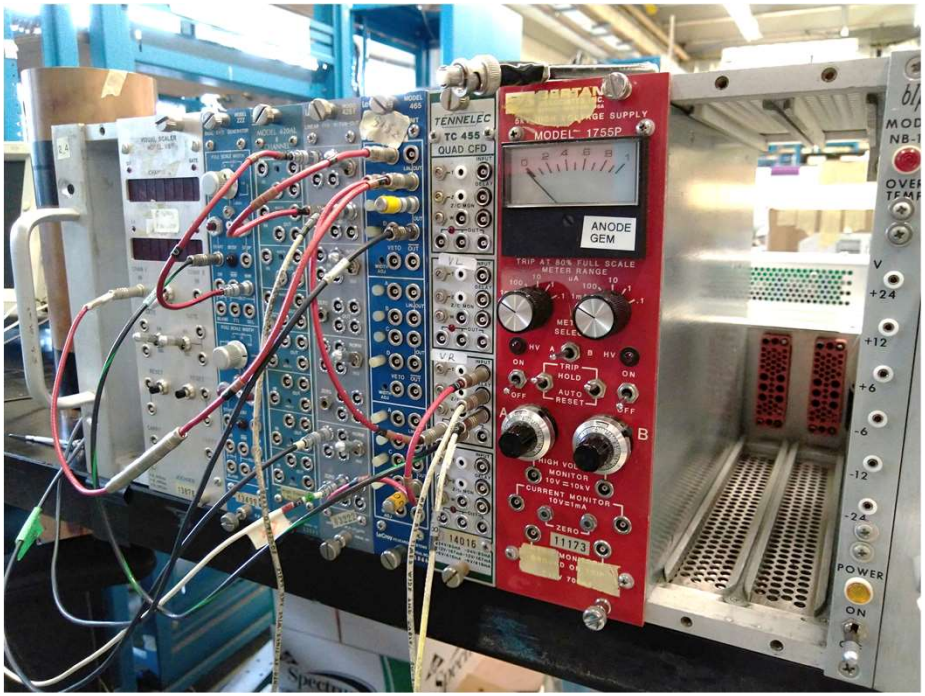
VXS (2006): VMEBus Switched Serial

- In use due to its serial bus backplane and slot configuration (Full mesh, Dual star). Redundant system (five-9 / max down time of 5.26 minutes per year.)

ATCA (uTCA) (2002): Advanced Telecommunications Computing Architecture

- PCI Industrial Computer Manufacturers Group (PICMG)
- New trend for Physics applications, combines VXS, self-managed crate, Single -48V, fully differential connections.

NIM (1968) : Nuclear Instrument Module (still in use)



Basic Analog elements:
Delay
Splitter
Discriminator
Attenuator
Pre-Amplifier

Basic Logic elements
Inverter AND, OR
Latch, Timer, Scaler

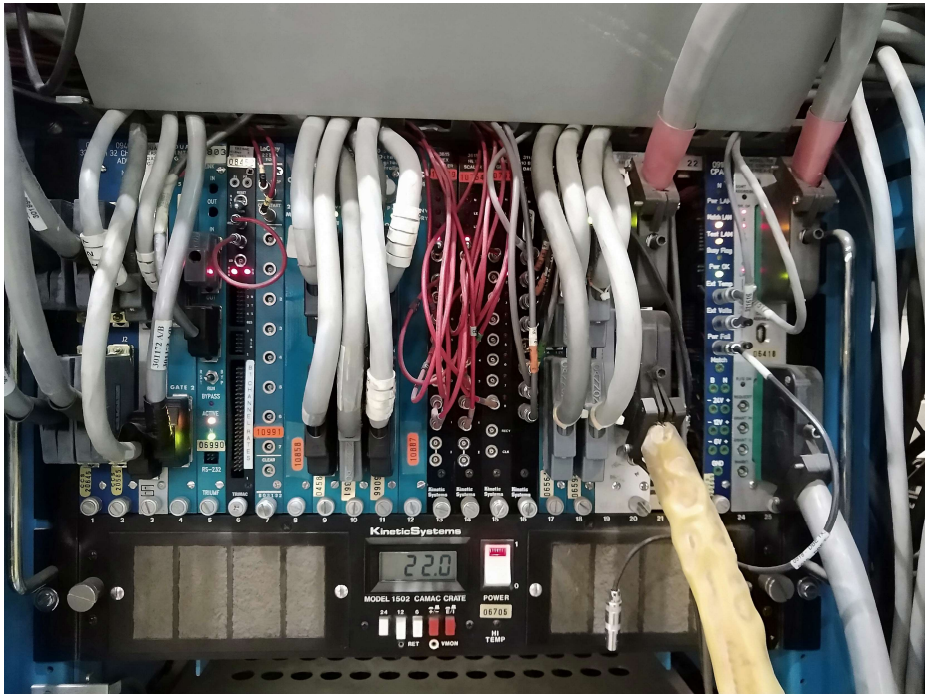
For
Power
+/- 6V
+/- 12V
+/-24V

CAMAC (1972) : Computer Automated Measurement and Control (found in older working systems)

Analog to Digital converter
Programmable…
Delays, Discriminators,
Attenuators, I/Os, etc…
ADC, TDC, Scalers…

For Power:
+/- 6V, +/- 12V, +/-24V
AC117V

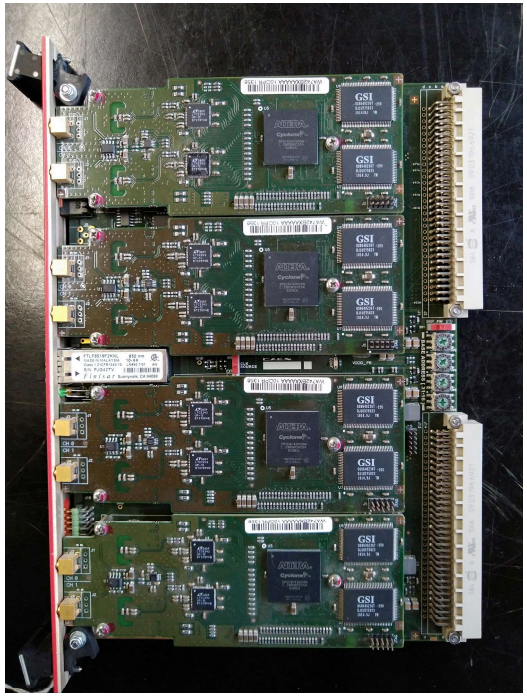
For Communication:
Slot Address N5
Module Add A4
Function bus F5
Data bus R24/W24



VME (1981) : Vesa Module Europcard (currently used in most physics labs)

FPGAs for Logic

VMEIO - 2009

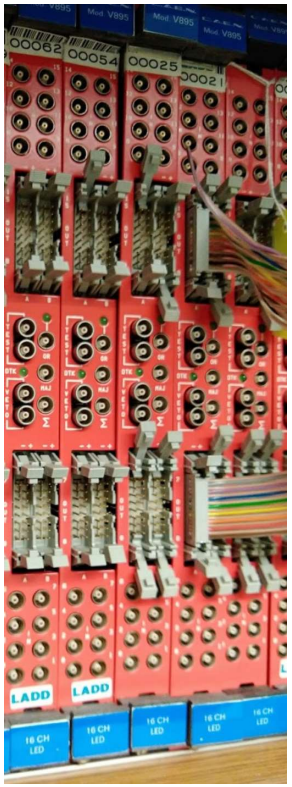


CAEN V1720 8ch, 12bits@250Msps

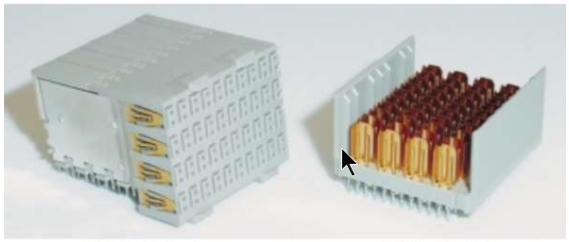
Analog to Digital converter
Programmable…
Delays, Discriminators,
Attenuators, I/Os, etc…
ADC, TDC, Scalers…

For Power:
+/- 5V, +/- 12V, +3.3V

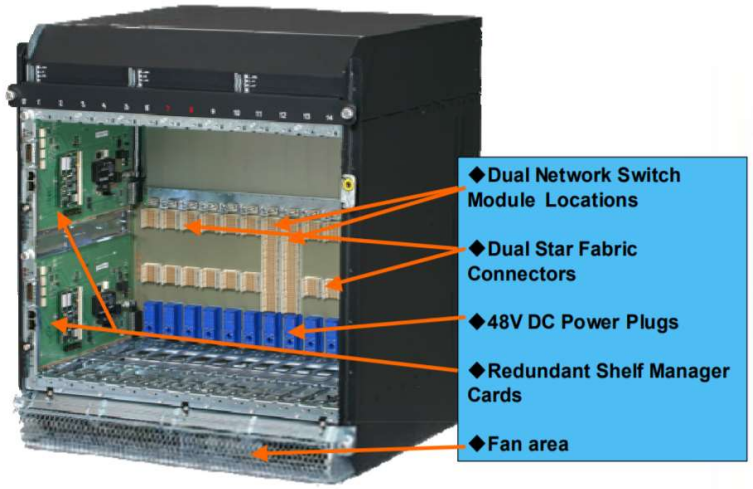
For Communication
Address Bus: A32
Data Bus: D32
Control bus: IRQ, AM5, AS, DS0/1, +…

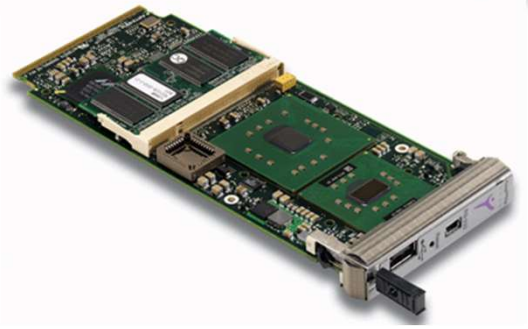


ATCA (uTCA): Advanced Telecommunications Computing Architecture (New large system choice)



Five nines means "99.999%",
High availability of services





Data Acquisition -

We have

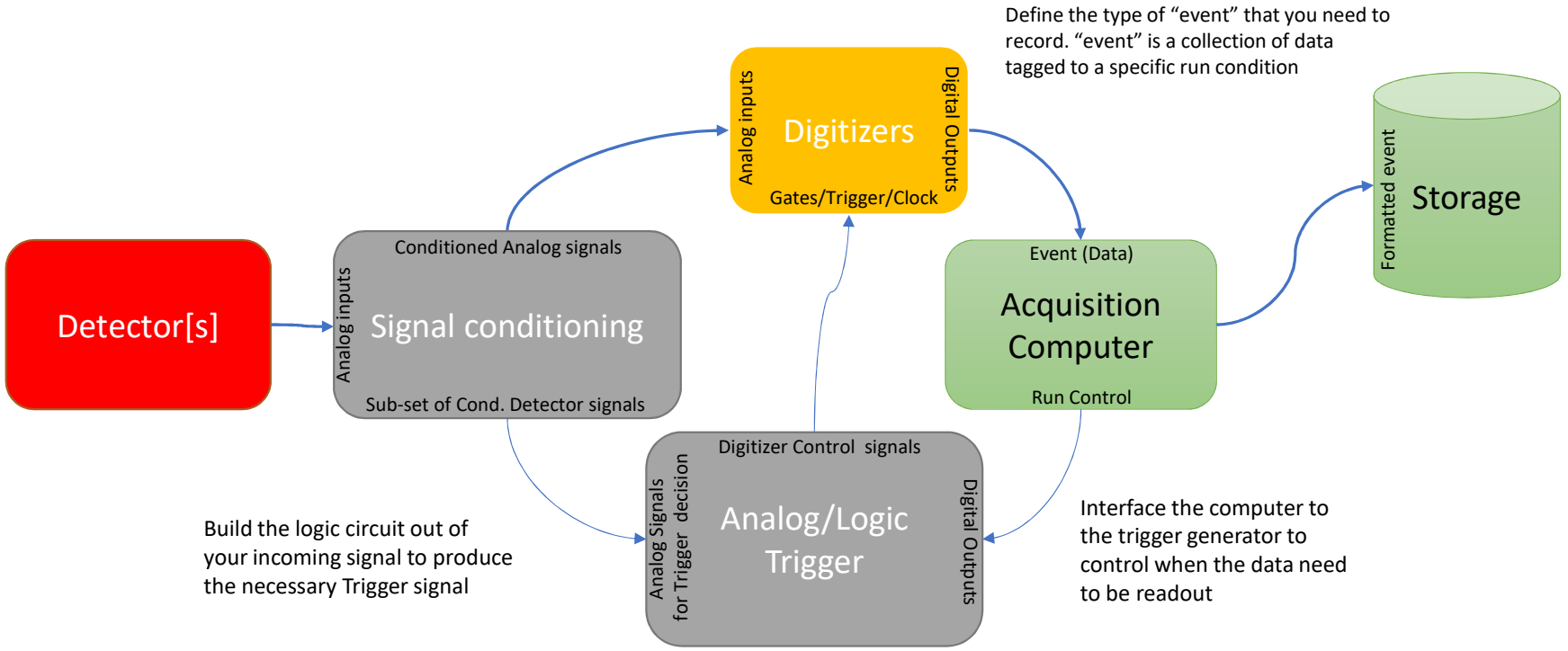
- A detector producing electrical signals
- Analog electronic circuitry to condition/shape the signal for the digitizers
- Digitizers for Amplitude, Charge, Time conversion

What do we want to do?

- Define the type of "event" that you need to record
  - "event": collection of data tagged to a specific condition
    - Two mode: "Triggered event" or "Triggerless data" (notion of time stamping the data)
    - Build the logic circuit out of your incoming signal to produce the necessary Trigger signal
    - Interface the computer to the trigger generator to control when the data need to be readout

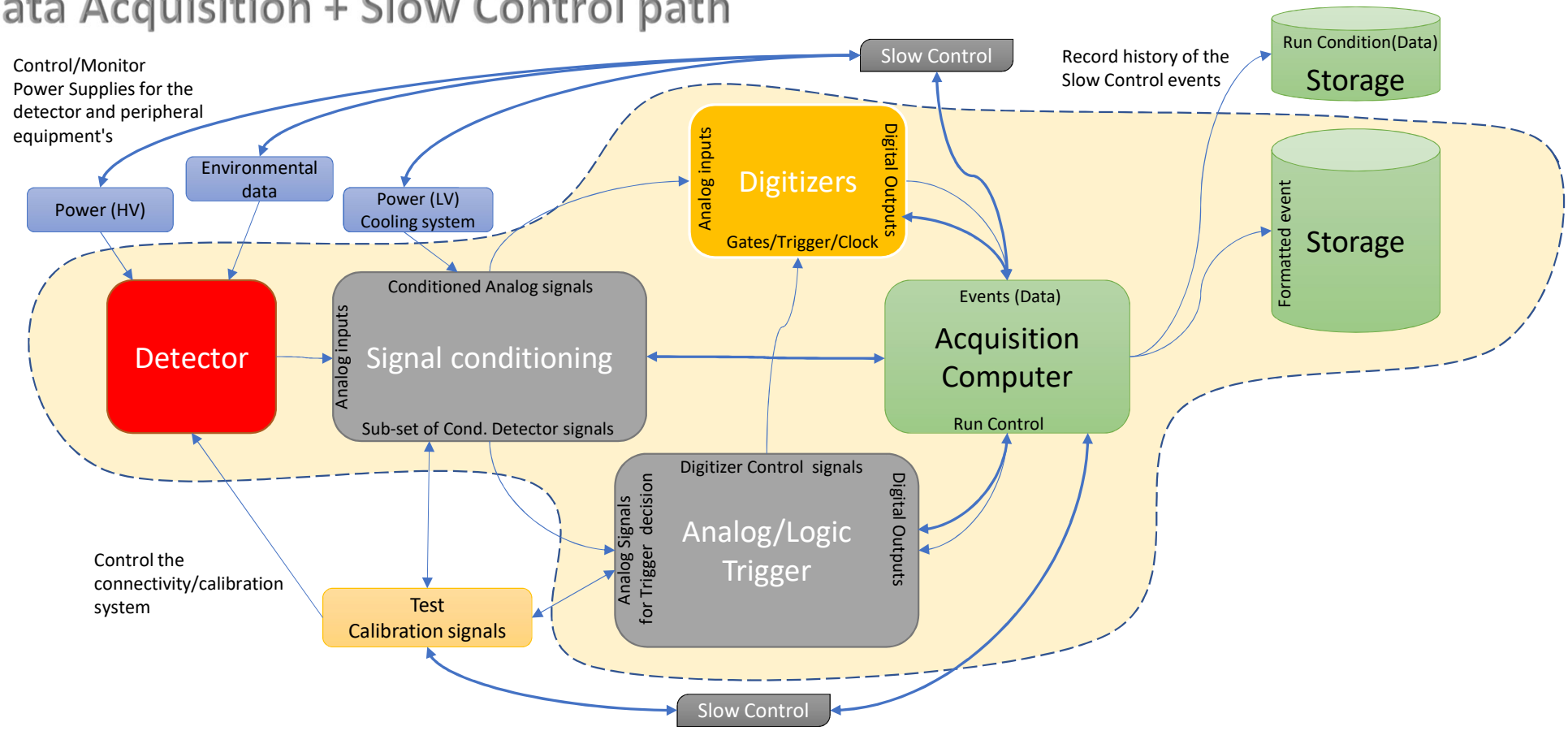
- Access to any hardware equipment involved in the DAQ for
  - Configuration
  - Reading the stored data (in the hardware equipment)

Data Acquisition – Physics Data path

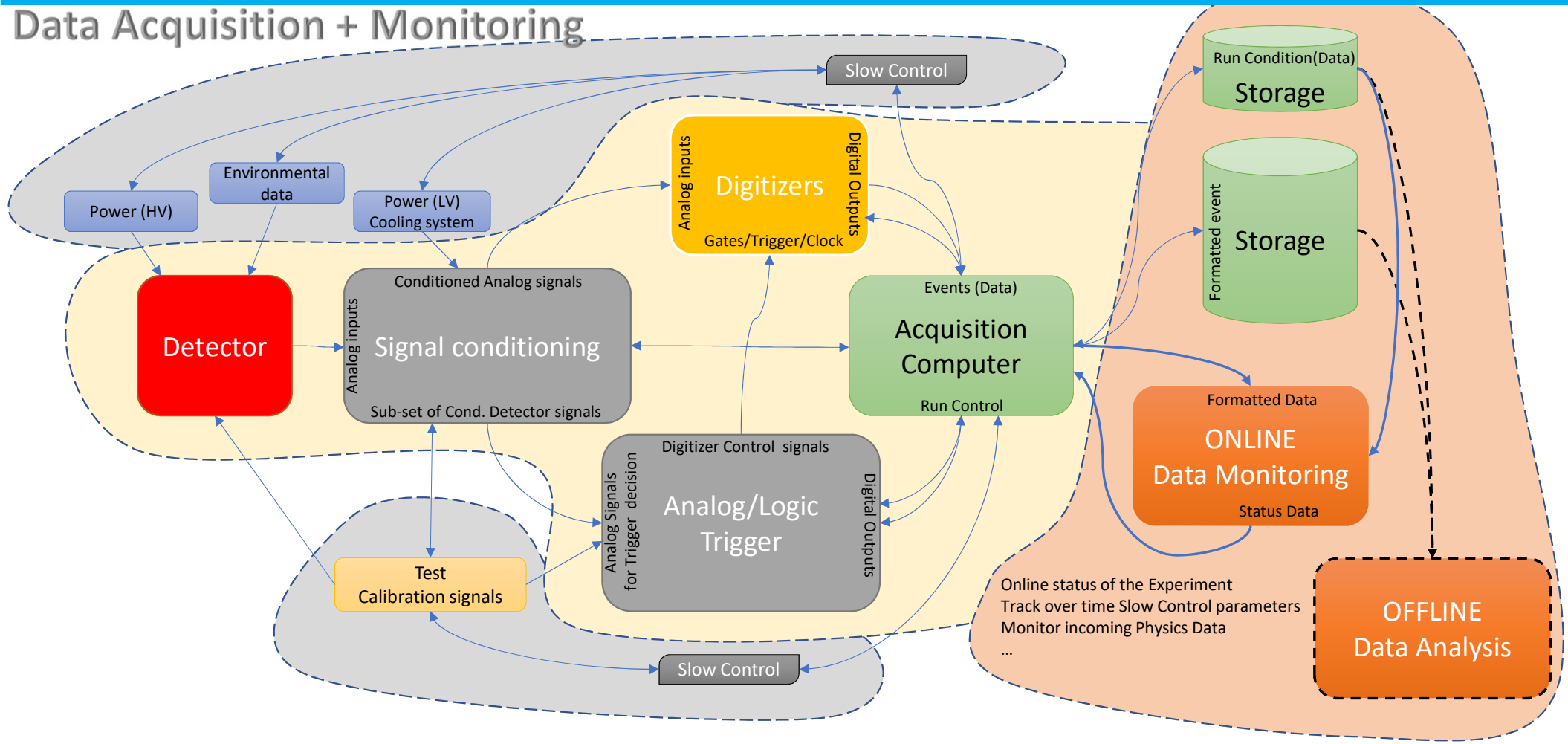


Digitizer may implement a crude DSP for Signal conditioning and simple trigger logic

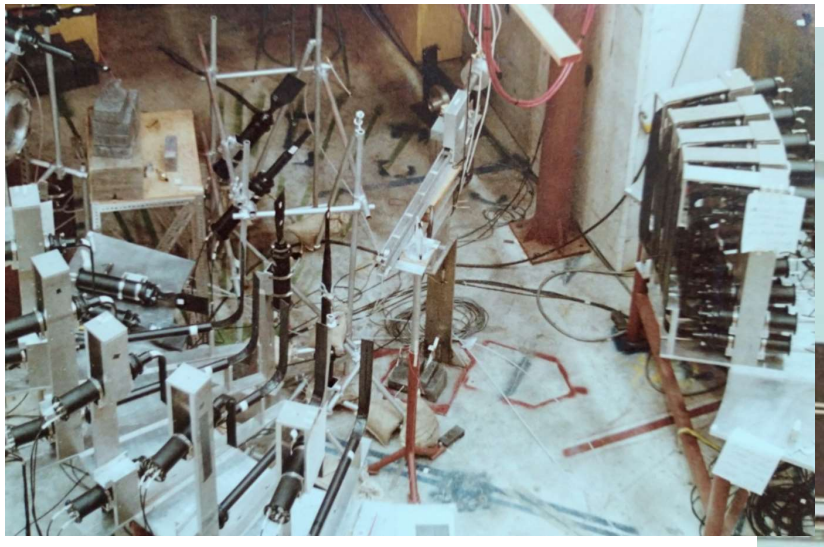
Data Acquisition + Slow Control path

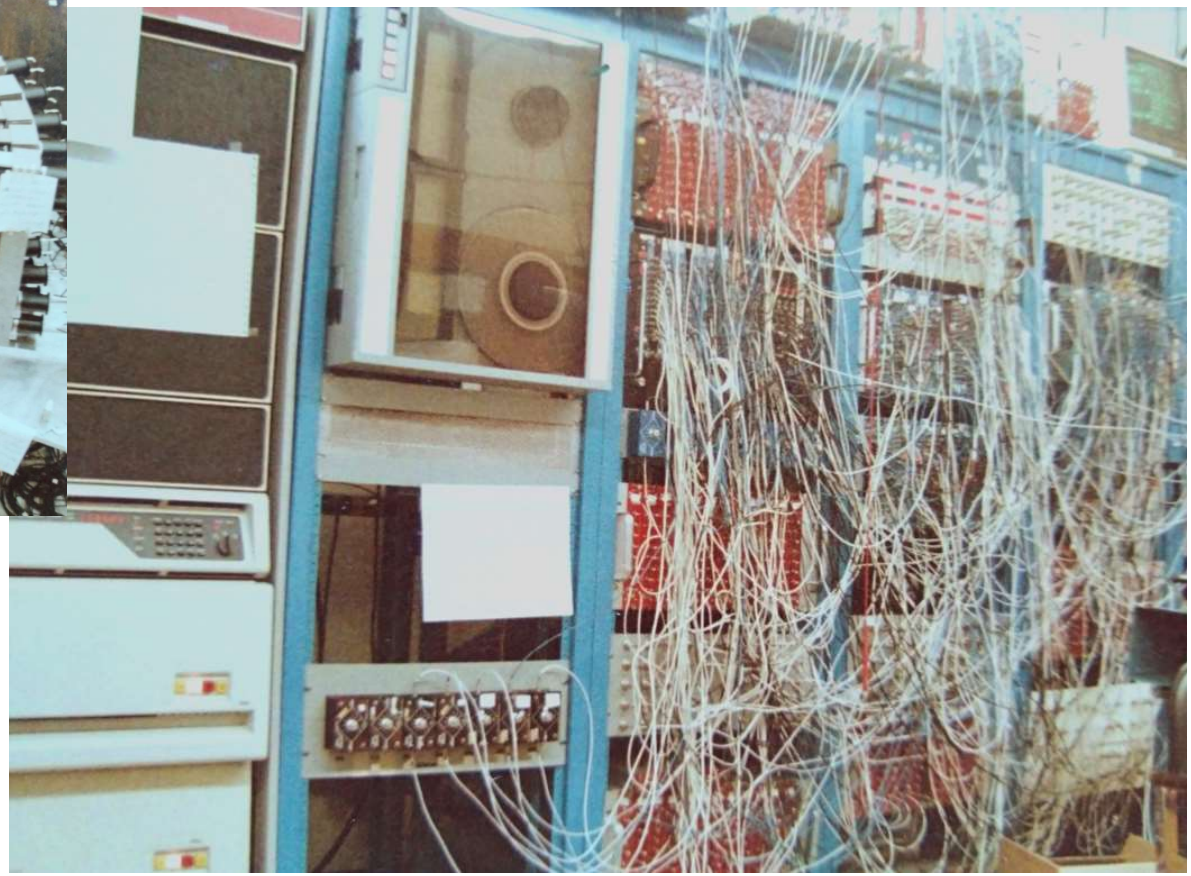


Data Acquisition + Monitoring



Experiment - examples - π-scat

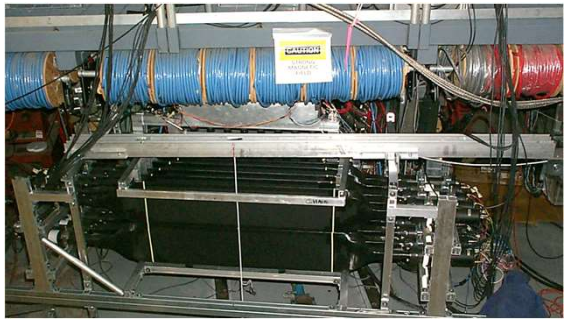


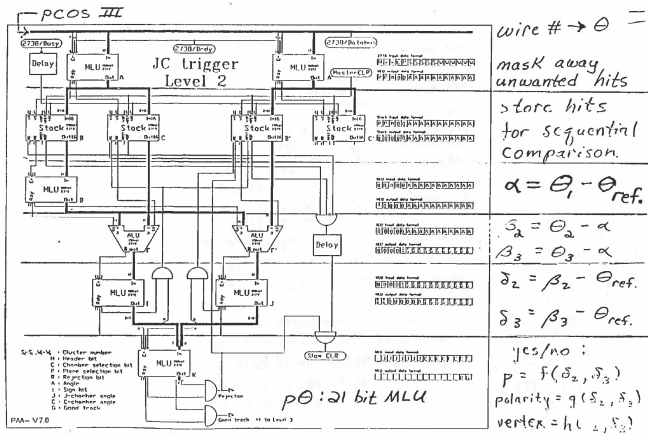


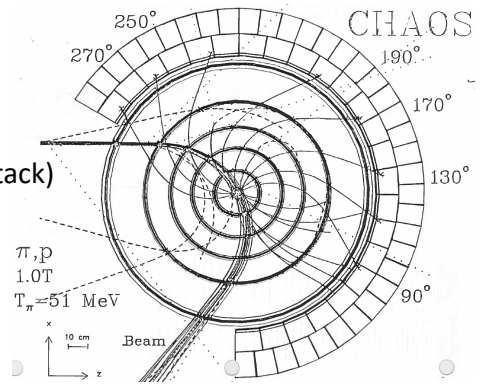
Period: < 1985
Channel Count: <100
DAQ Hardware: NIM, CAMAC [ADCs, TDCs, Scalers]
Computer: Digital PDP 11/34
Rates: 100evt/s
Programming Language: FORTRAN
Storage: Memorex MRX-V ½"x 10-¾"

Experiment - examples - CHAOS

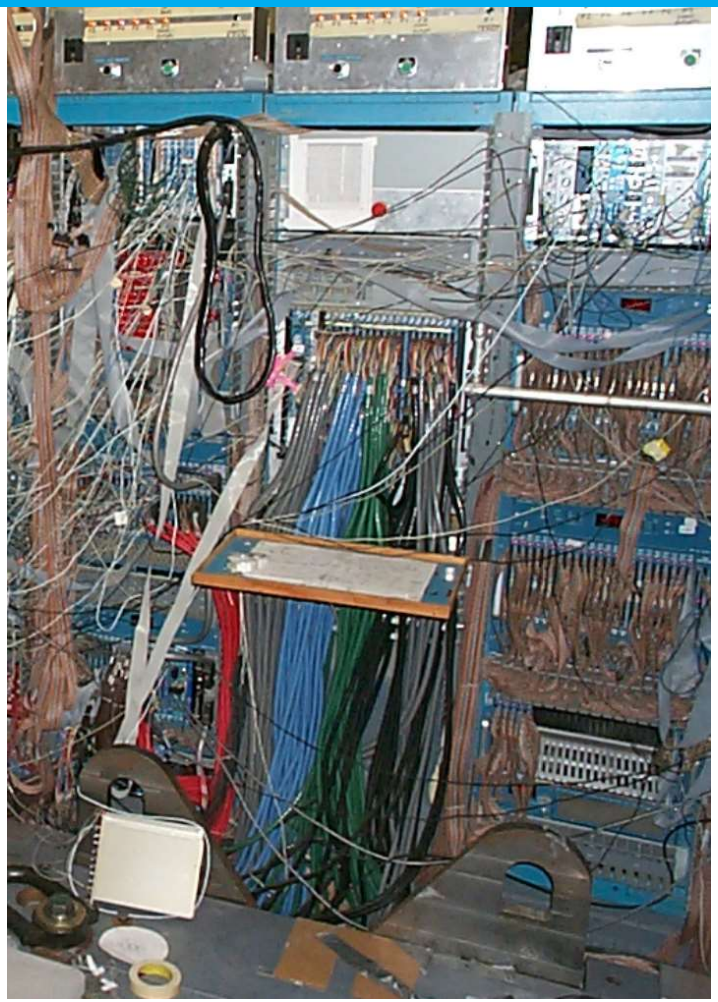
Delay Lines (~20m) for ~2000 channels



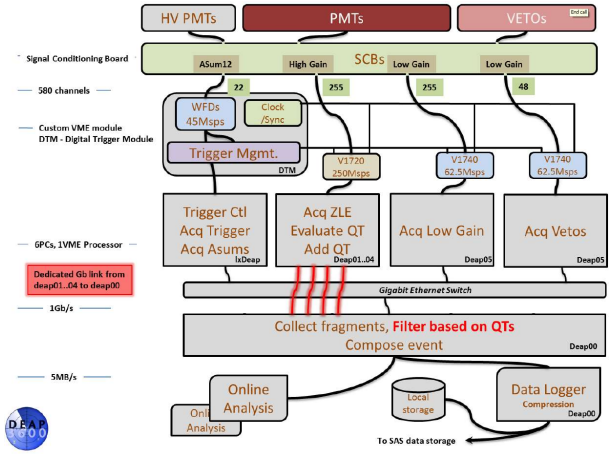


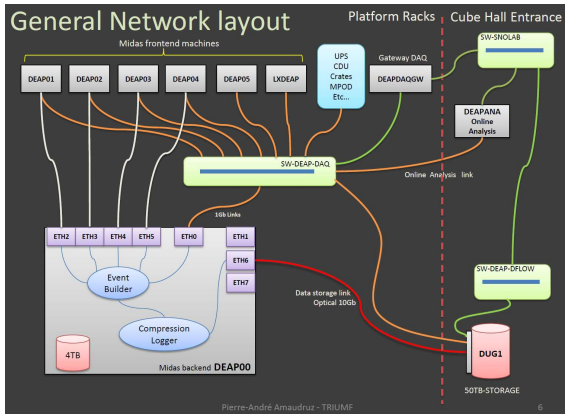


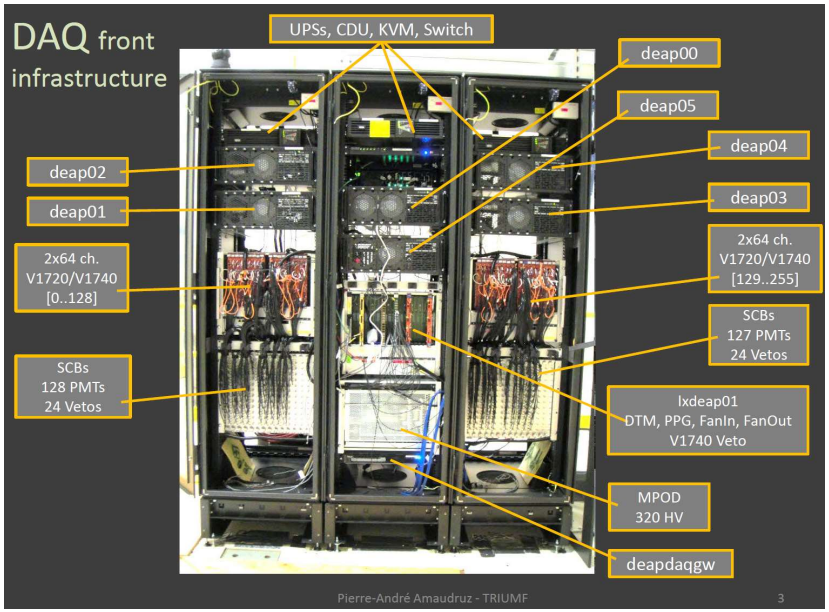
Period: 1990 - 2000
Channel Count: ~2500
DAQ Hardware: NIM, CAMAC, VME, FastBus
L2-Trigger **FPGA Precursor** in ECL-logic (CAMAC: ALU, MLU, Stack)
Computer: Digital µVax-3400
Rates: few hundred events per second
Programming Language: FORTRAN
Storage: Sony QG112M 2.5/5GB 8mm D8 Data Cartridge
DLTape IV 80GB (compressed)



Experiment - examples - DEAP

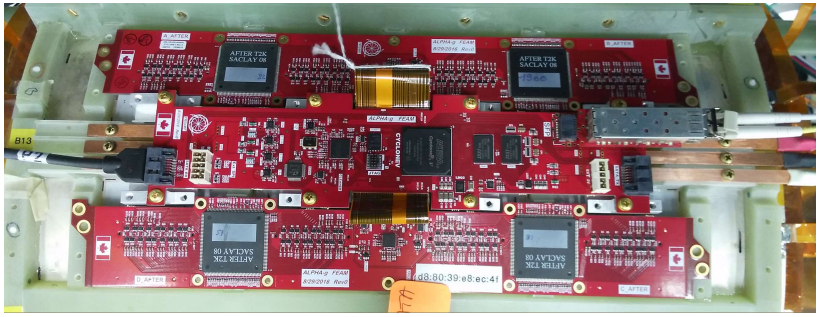




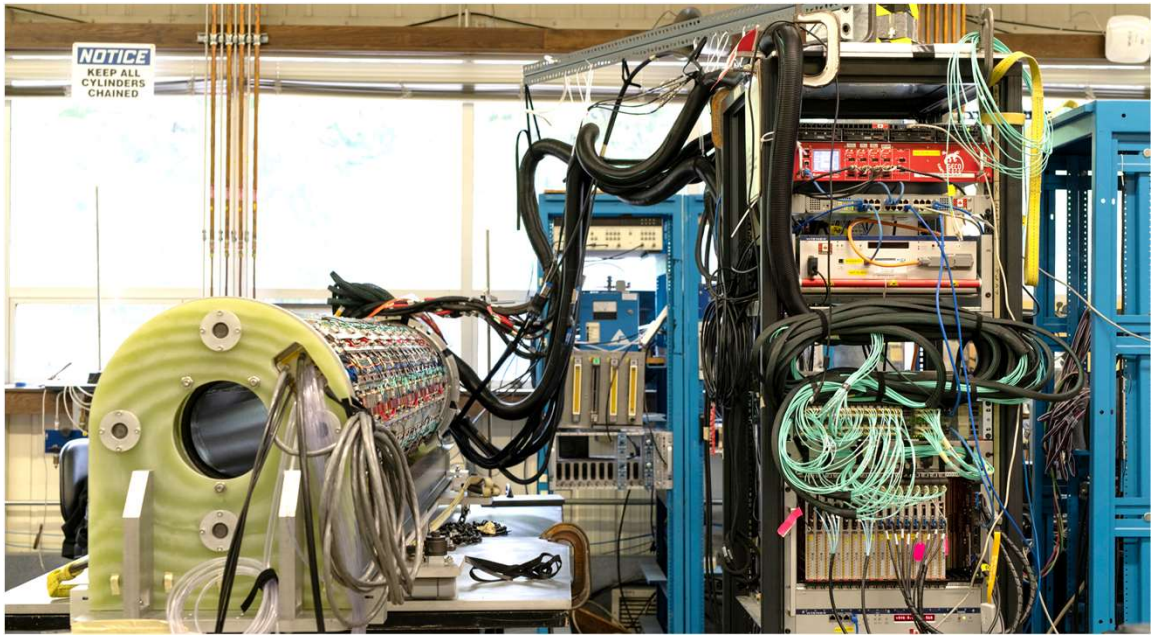


Period: 2010 -
Channel Count: ~600
DAQ Hardware: VME, PCIe Optical interface
L1 Trigger FPGA-based
Computer: PCs
Rates: ~3KEvt/s, ~12MB/s
Programming Language: C, C++, Web tools
Storage: Local HDD, Cloud

Experiment - examples - Alpha-g

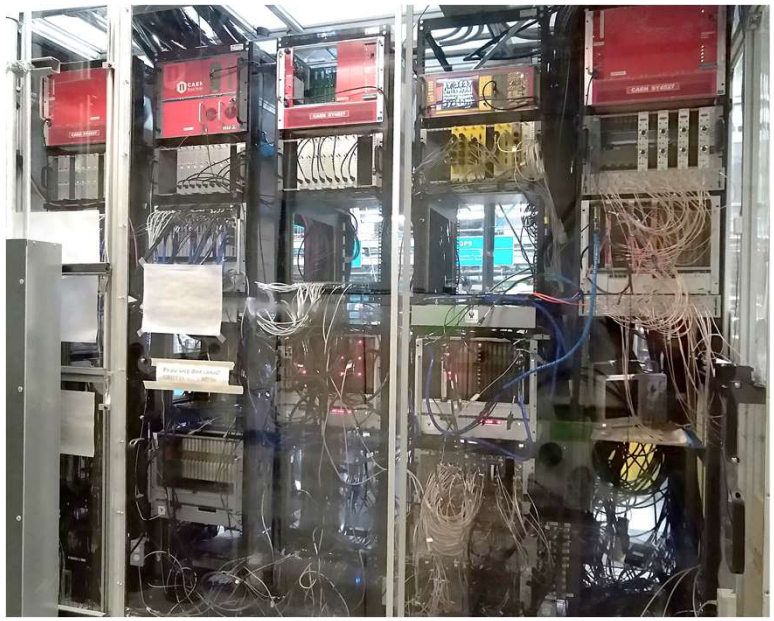


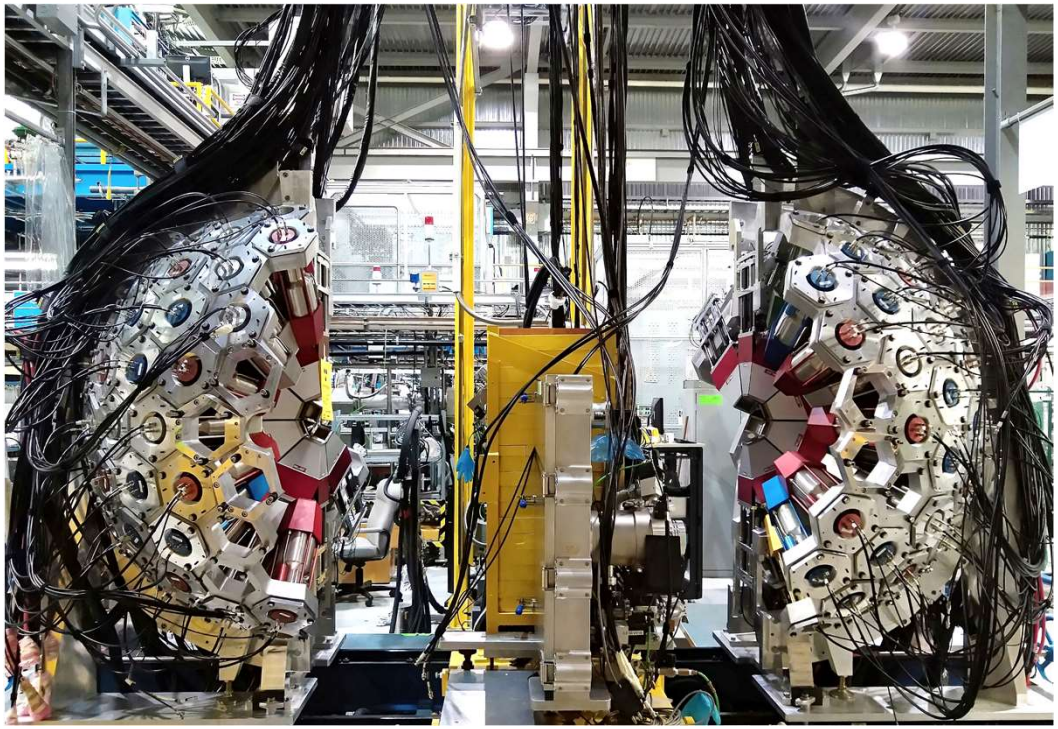
Period: 2016 -
Channel Count: ~19'000! … (18'000 of SCAs)
DAQ Hardware: VME (for power only), Ethernet Optical Links
Custom Build Hardware with FPGAs : WFDs, TDCs, Logic
Computer: PCs
Rates: ~1KEvt/s, ~200MB/s
Programming Language: C, C++, Web tools
Storage: Local HDD, Cloud



Large portion of the frontend electronics including the waveform digitizers reside on the detector (256 ASICs)

Experiment - examples - GRIFFIN





Period: 2013 - …
Channel Count: ~500
DAQ Hardware: NIM, VME (for power only), Ethernet Links
FPGA Custom Build Hardware: WFDs, Logic
Computer: PCs, 1, 10Gb Ethernet
Rates: ~3KEvt/s, 120MB/s
Programming Language: C, C++, Web tools
Storage: Local HDD

Data Acquisition - Status

What features the DAQ system should provide?

- Run Control

  Define the data acquisition sequence – Run concept (cycle) –

  Run: Data set collected during a defined experimental condition.
- Record the selected Data to storage device

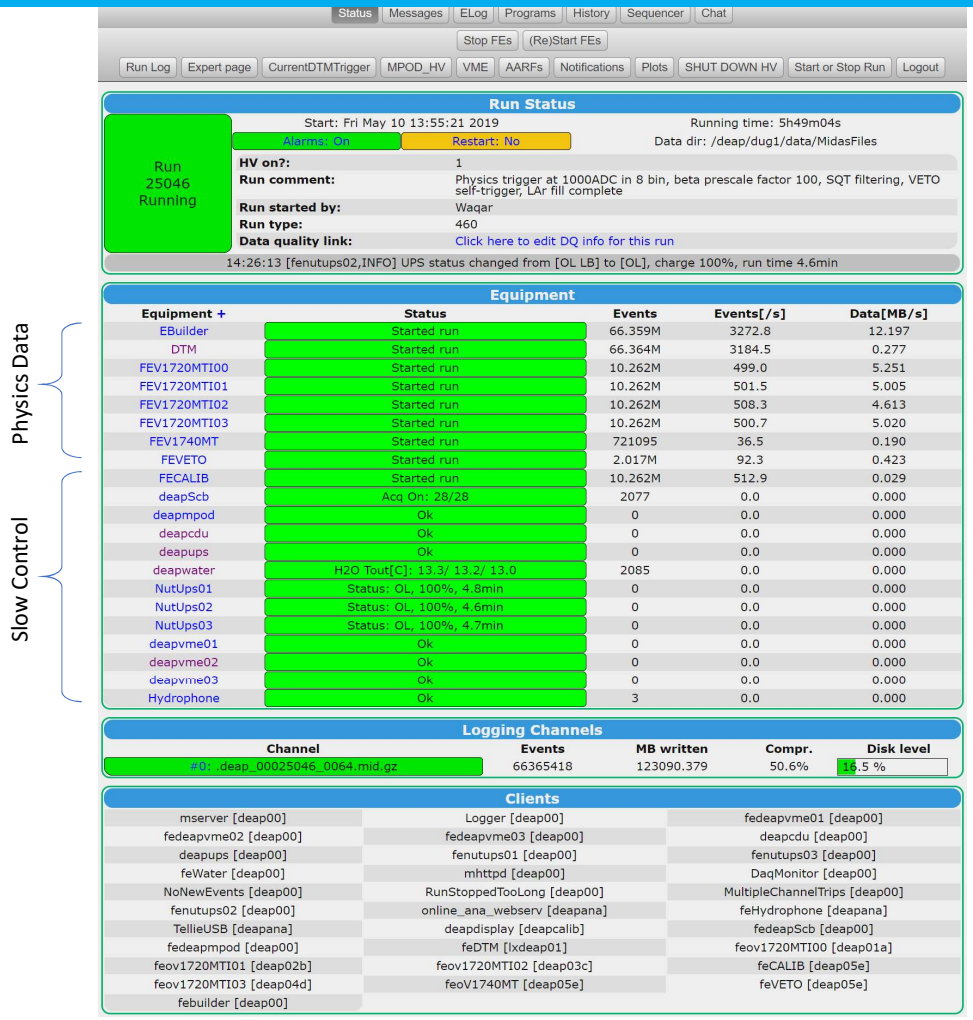
  Multiple storage media, event type, etc. (Logger)
- Hardware configuration

  Based on pre-selected configuration
- Online status of the Experiment

  Real time messages with permanent record (log)
- Track over time experimental condition parameters

  Chart plot of any experimental variable (History)
- Monitor incoming Physics Data

  Online Data Analysis mechanism with data display (Rootana)
- Custom User Parameters/Data display (Custom Web page, script)
- Custom alarm and custom action based on Alarm condition (Alarms)
- And more…



Data Acquisition - Status-II

Current DTM Trigger Settings

Main DAQ Page

Active DTM Triggers (both trigger output and trigger source are enabled)

Trigger output					Trigger source	
ID	Output mask	ADC type	Delay	Prescale factor	ID	Type
0x1	0x8 (Veto)	0x1 (Summary)	1	1	0x80	External
0x2000	0x12 (V1720, Calib)	0x1 (Summary)	1	1	0x400	ADC trigger (E_low, F_low)
0x4000	0x0	0x6 (Channels, Sum)	1	1000	0x400	ADC trigger (E_low, F_low)
0x8000	0x12 (V1720, Calib)	0x1 (Summary)	1	1	0x800	ADC trigger (E_low, F_high)
0x10000	0x0	0x6 (Channels, Sum)	1	1000	0x800	ADC trigger (E_low, F_high)
0x20000	0x16 (V1720, V1740, Calib)	0x1 (Summary)	1	100	0x1000	ADC trigger (E_high, F_low)
0x40000	0x0	0x6 (Channels, Sum)	1	5000	0x1000	ADC trigger (E_high, F_low)
0x80000	0x16 (V1720, V1740, Calib)	0x1 (Summary)	1	1	0x2000	ADC trigger (E_high, F_high)
0x100000	0x0	0x6 (Channels, Sum)	1	1000	0x2000	ADC trigger (E_high, F_high)
0x200000	0x16 (V1720, V1740, Calib)	0x1 (Summary)	1	1	0x4000	ADC trigger (E_very_high)
0x400000	0x0	0x6 (Channels, Sum)	1	1000	0x4000	ADC trigger (E_very_high)
0x800000	0x0	0x1 (Summary)	1	1	0x1000	ADC trigger (E_high, F_low)
0x40000000	0x20 (DNF)	0x6 (Channels, Sum)	1	40	0x2	Periodic, 40Hz
0x80000000	0x1a (V1720, Veto, Calib)	0x1 (Summary)	1	1	0x2	Periodic, 40Hz

Copy settings for elog | Add standard trigger for monitoring dark noise rates | Add standard trigger for PPG | Set suppression time to 2000

Hex calculator

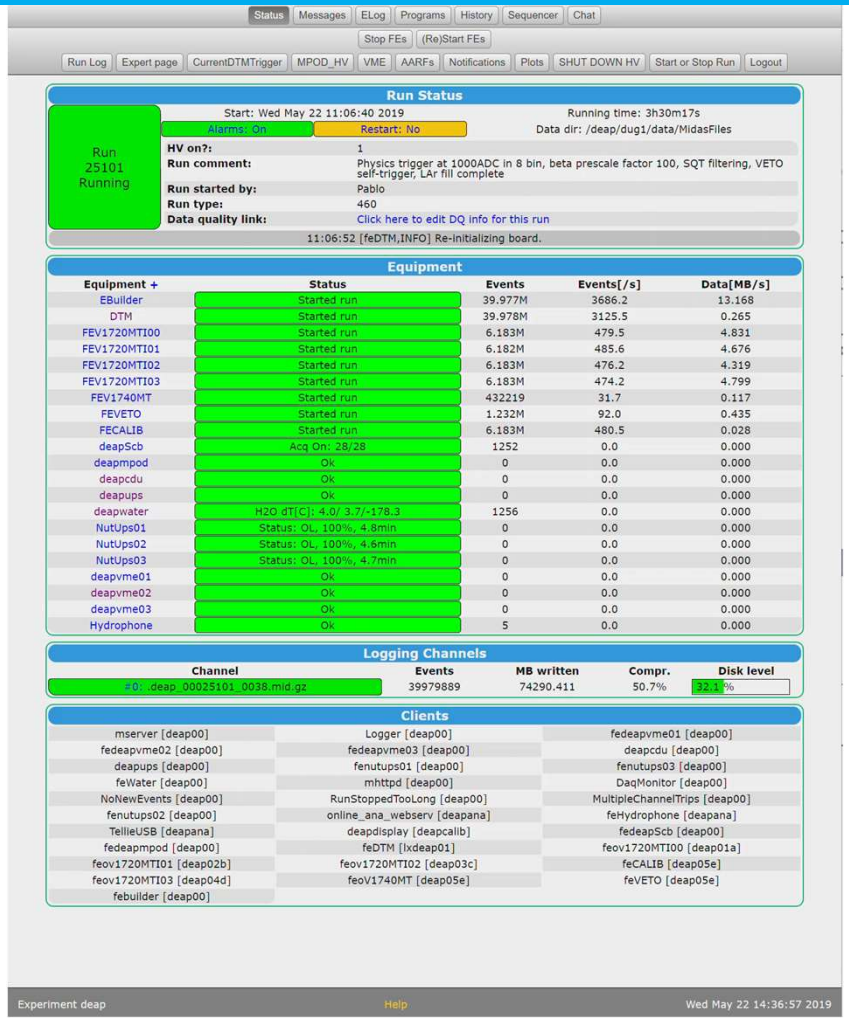
Bit	0	1	2	3	4	5	6	7	= 0x0
Output mask	PPG	V1720	V1740	Veto	Calib	DNF	AARF	NIM 7	
ADC type	Summary	Channels	Sum						

Event Builder Fragments Enabled

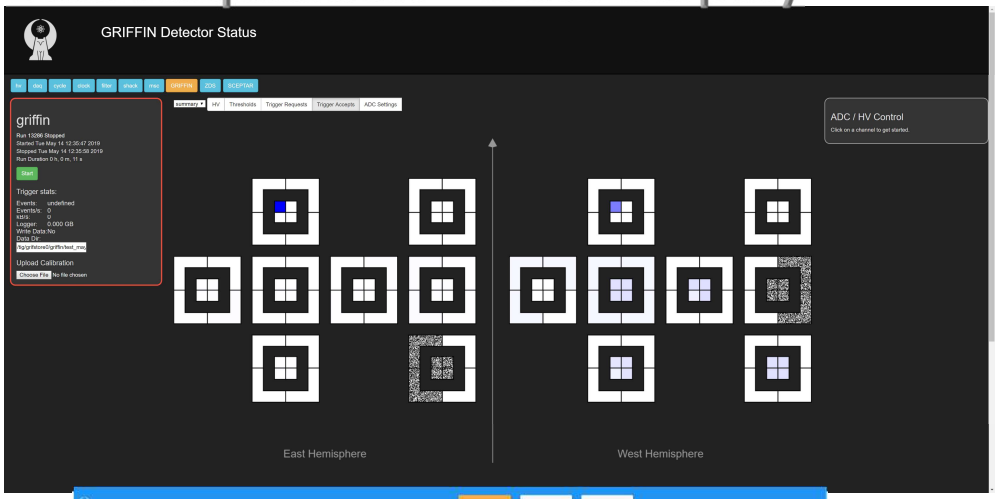
V1720-0 (y) V1720-1 (y) V1720-2 (y) V1720-3 (y) V1740 (y) Veto (y) Calib (y)

Last updated Fri May 10 2019 17:00:54 GMT-0700 (Pacific Daylight Time)

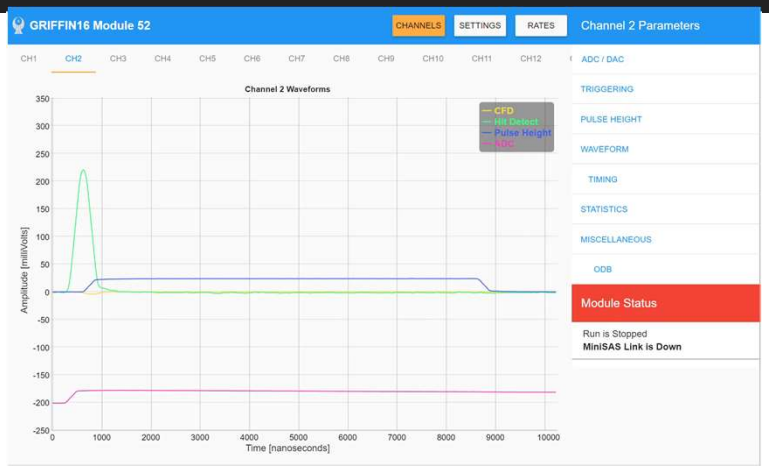
Javascript executed in 465 ms.

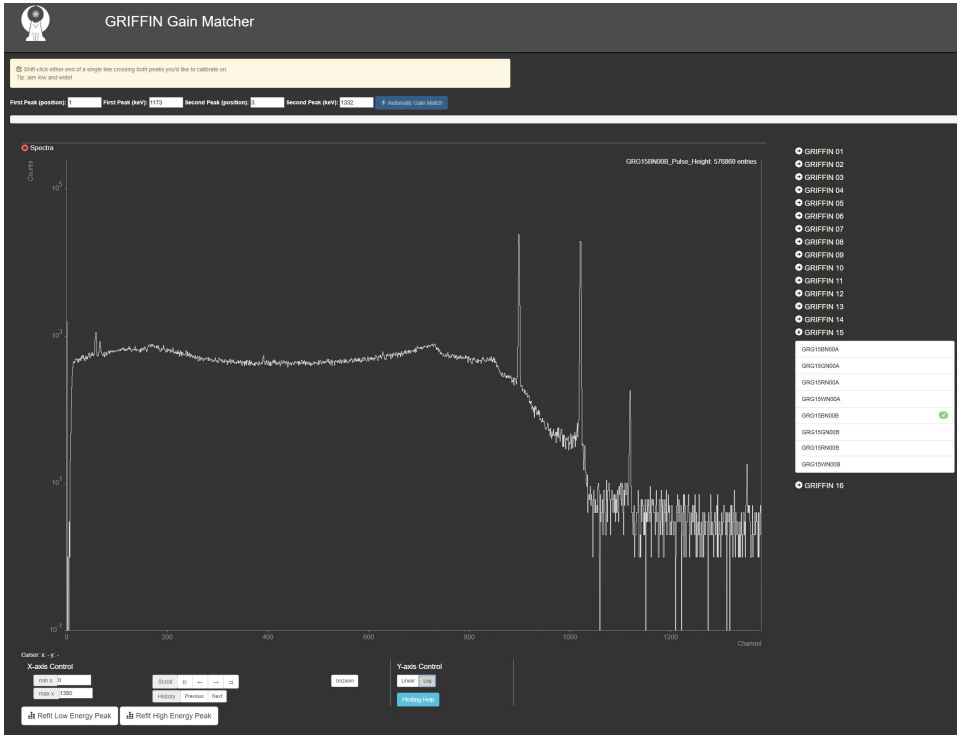


Data Acquisition – Data Display



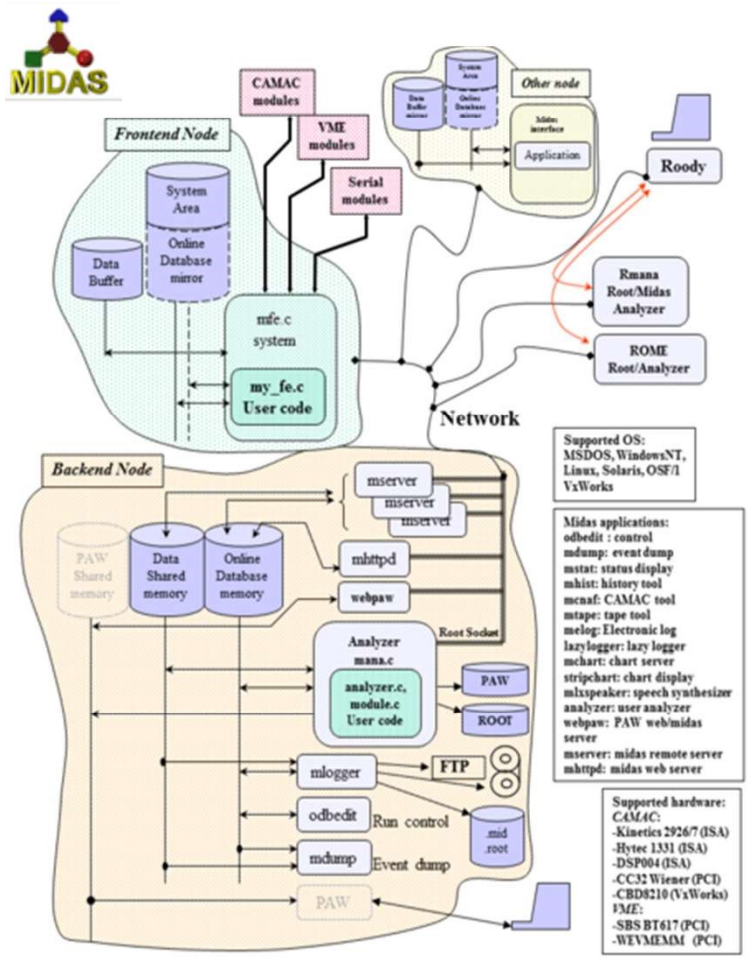
Detector Status: HV, Threshold, Rate, Settings



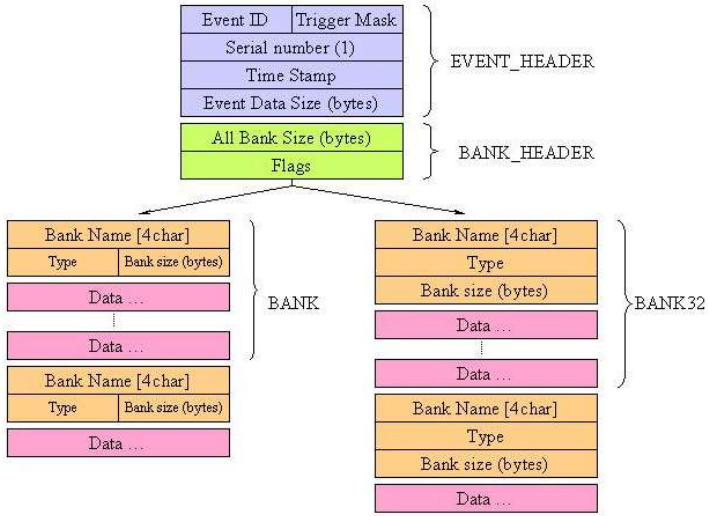


Detector Status: Spectrum

Data Acquisition – Software Architecture



Midas Data Structure




```
Evid:0001- Mask:0002- Serial:39036- Time:0x5c5cd9c2- Dsize:512376/0x7d178
#banks:4 - Bank list:-W200W201W202W203-

Bank:W200 Length: 128080(I*1)/32020(I*4)/32020(Type) Type:Unsigned Integer*4
   1-> 0xa0007d14 0x000002ff 0xff00987c 0x1bc43d3d 0x3aa707d1 0x3aa33aa6 0x3aa63aa4 0x3aa53aa7
   9-> 0x3aa73aa9 0x3aa63aab 0x3aac3aa2 0x3aa63aa7 0x3aa73aa2 0x3aa43aa4 0x3aa73aa9 0x3aa93aa7
  17-> 0x3aa63aa1 0x3aab3aa5 0x3aa33aa4 0x3aa83aa5 0x3aab3aa7 0x3aa83aa3 0x3aa53aa6 0x3aa73aa5
  25-> 0x3aaa3aa4 0x3aa83aa2 0x3aa63aa5 0x3aa83aa9 0x3aab3aa6 0x3aaa3aa9 0x3aaa3aa2 0x3aa73aa3
  33-> 0x3aaa3aa7 0x3aa53aa6 0x3aab3aa6 0x3aa53aa6 0x3aa63aa2 0x3aa53aa5 0x3aa93aa1 0x3aa93aa5
  41-> 0x3aa53aa5 0x3aaa3aa5 0x3aa53aa1 0x3aa73aa4 0x3aa43aa6 0x3aaa3aa7 0x3aa53aa2 0x3aac3aa7
```

Data Acquisition - Code

Function Templates

```
/********************************************************************\
              Callback routines for system transitions

  These routines are called whenever a system transition like start/
  stop of a run occurs. The routines are called on the following
  occasions:

  frontend_init:  When the frontend program is started. This routine
                  should initialize the hardware.

  frontend_exit:  When the frontend program is shut down. Can be used
                  to release any locked resources like memory,
                  communications ports etc.

  begin_of_run:   When a new run is started. Clear scalers, open
                  run gates, etc.

  end_of_run:     Called on a request to stop a run. Can send
                  end-of-run event and close run gates.

  pause_run:      When a run is paused. Should disable trigger events.

  resume_run:     When a run is resumed. Should enable trigger events.
\********************************************************************/
```

Equipment: Sub-set of the data composing the event

```
EQUIPMENT equipment[] = {

   {"Trigger",              /* equipment name */
      {1, 0,                /* event ID, trigger mask */
         "SYSTEM",          /* event buffer */
         EQ_POLLED,         /* equipment type */
         0,                 /* event source */
         "MIDAS",           /* format */
         TRUE,              /* enabled */
         RO_RUNNING |       /* read only when running */
         RO_ODB,            /* and update ODB */
         100,               /* poll for 100ms */
         0,                 /* stop run after this event limit */
         0,                 /* number of sub events */
         0,                 /* don't log history */
         "", "", "",},
      read_trigger_event,   /* readout routine */
   },

   {"Periodic",             /* equipment name */
      {2, 0,                /* event ID, trigger mask */
         "SYSTEM",          /* event buffer */
         EQ_PERIODIC,       /* equipment type */
         0,                 /* event source */
         "MIDAS",           /* format */
         TRUE,              /* enabled */
         RO_RUNNING | RO_TRANSITIONS |   /* read when running and on transitions */
         RO_ODB,            /* and update ODB */
         1000,              /* read every sec */
         0,                 /* stop run after this event limit */
         0,                 /* number of sub events */
         TRUE,              /* log history */
         "", "", "",},
      read_periodic_event,  /* readout routine */
   },

   {""}
};
```

Readout Function

```
///-------------------------------
/* create structured ADC2 bank */
bk_create(pevent, "ADC2", TID_DWORD, &pdata);
/* Read Event */
v792_EventRead(myvme, VADC2_BASE, pdata, &nentry);
pdata += nentry;
bk_close(pevent, pdata);
```

Specific software driver to acquire the data from the hardware module.
VME, Ethernet, GPIB, RS-232
I2C, SPI, CANBus, etc…

There are other DAQ options?

- Most of the Physics Labs have their own DAQ system and experts.
- **Labview**: works well for many small setups
  - Labview drivers provided for many commercial devices.
  - Getting generic device drivers for linux can be tricky.
- **ORCA**: developed by group at University of North Carolina
  - Runs on MacOS
  - Experiments: KATRIN, MAJORANA, SNO+
- **Artdaq**: developed by FNAL
  - Based on art offline analysis framework (originally from CMS)
  - Experiments: LARiAT, Darkside-50, Mu2E
- **Midas-UK**: **M**ulti **I**nstance **D**ata **A**cquisition **S**ystem (Rutherford - STFC)
- **CODA** : Jefferson Laboratory (formerly **C**EBAF **O**nline **D**ata **A**cquisition)
- And many more…

Things to consider

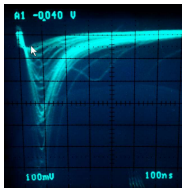
- Trigger – or – No Trigger (triggerless) system is an important aspect of the DAQ

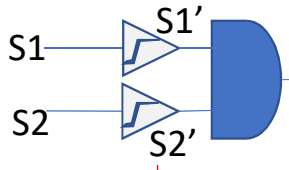
- Time synchronization is essential for large distributed DAQ systems
  - Single Global clock source distributed to all the acquisition hardware components

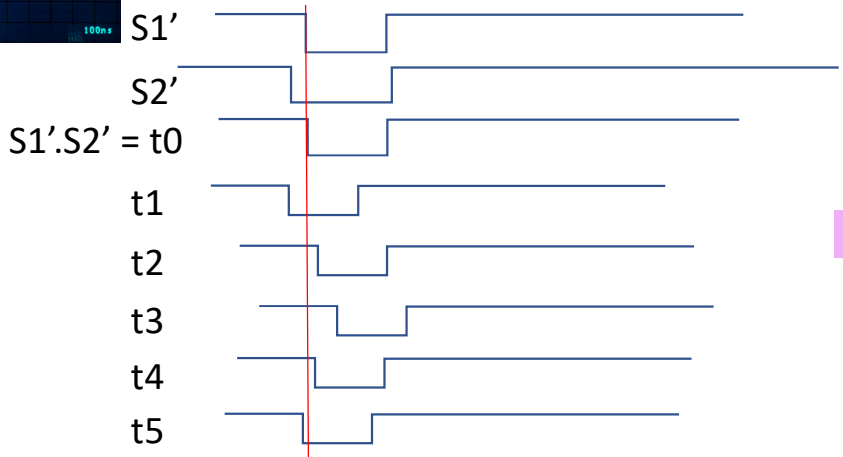
- Slow Control **is** part of the Data Acquisition System
  - Environment parameters, equipment monitoring, calibration system have to be included.
  - As the DAQ manage the whole electronic chain, consider separate path for data & power for slow control operation

- Don't underestimate thermal effect on the electronics equipment
  - Heat dissipation, necessity of a cooling system (air, water)
  - High current through contacts (power connectors current rating!)

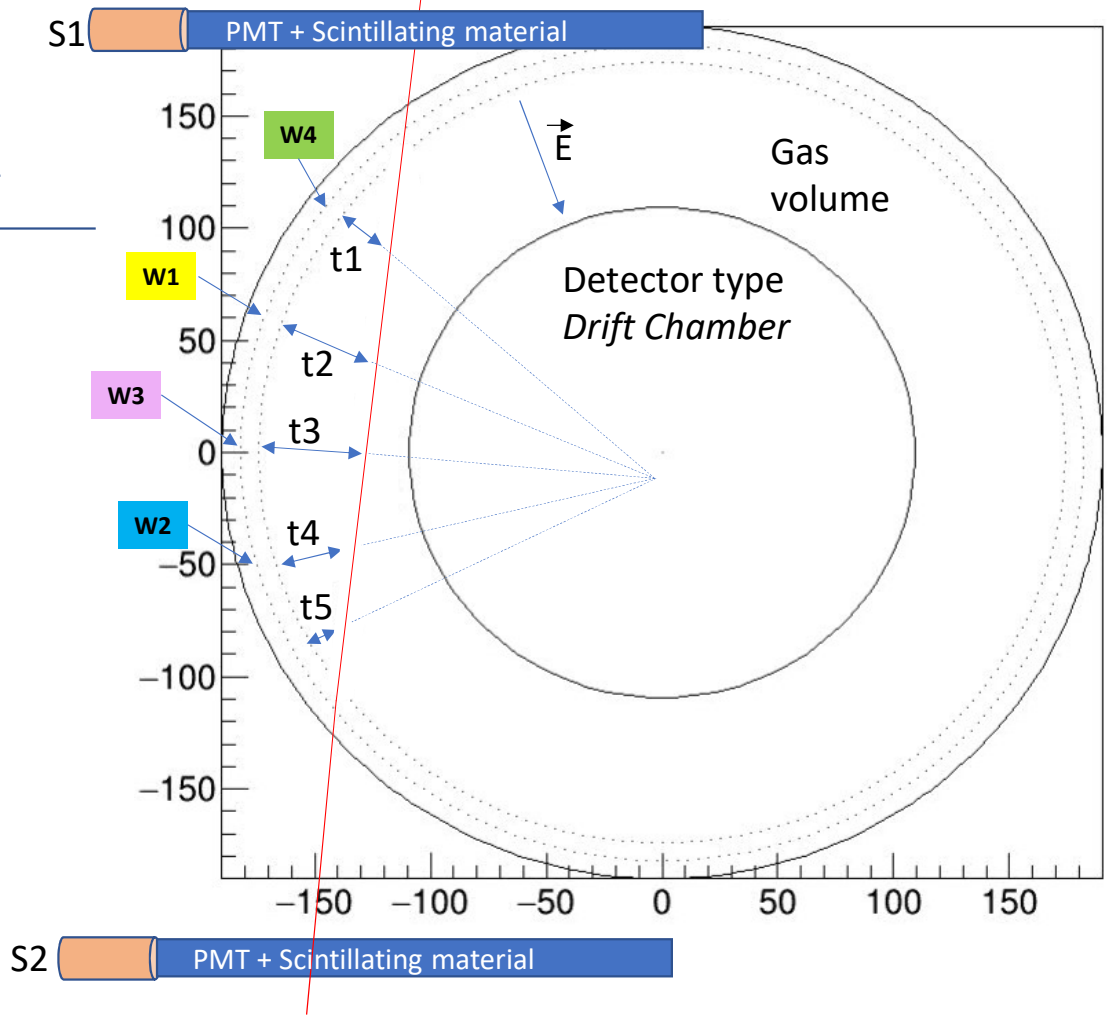
- Cable path organization facilitate channel recognition, module extraction (cable tray, please use GOOD label material!)

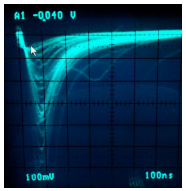



S1
S2
S1'
S2'
t0

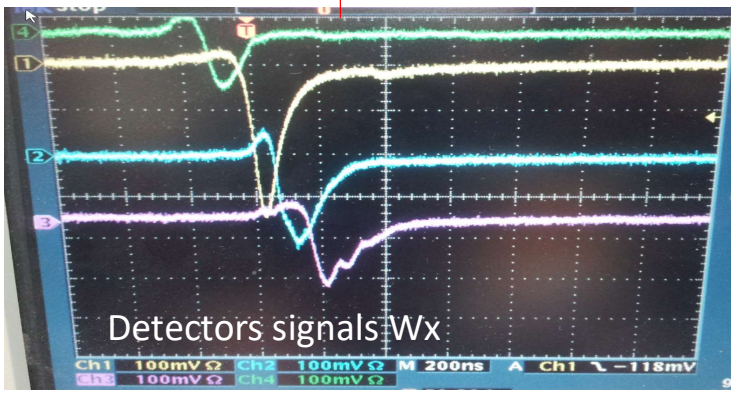

S1'
S2'
S1'.S2' = t0
t1
t2
t3
t4
t5

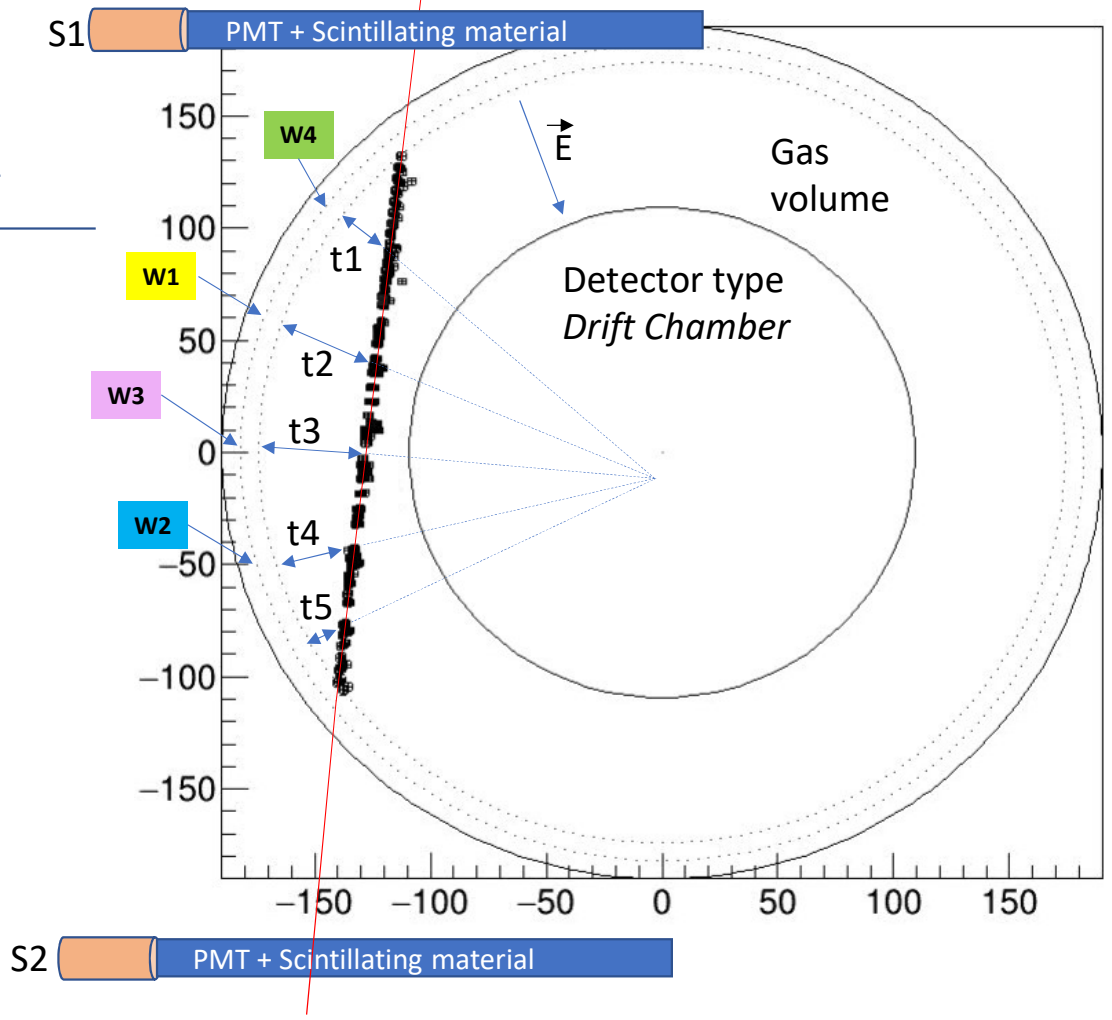

Detectors signals Wx


S1
PMT + Scintillating material
W4
W1
W3
W2
E
Gas volume
Detector type
Drift Chamber
t1
t2
t3
t4
t5
150
100
50
0
−50
−100
−150
−150 −100 −50 0 50 100 150
S2
PMT + Scintillating material

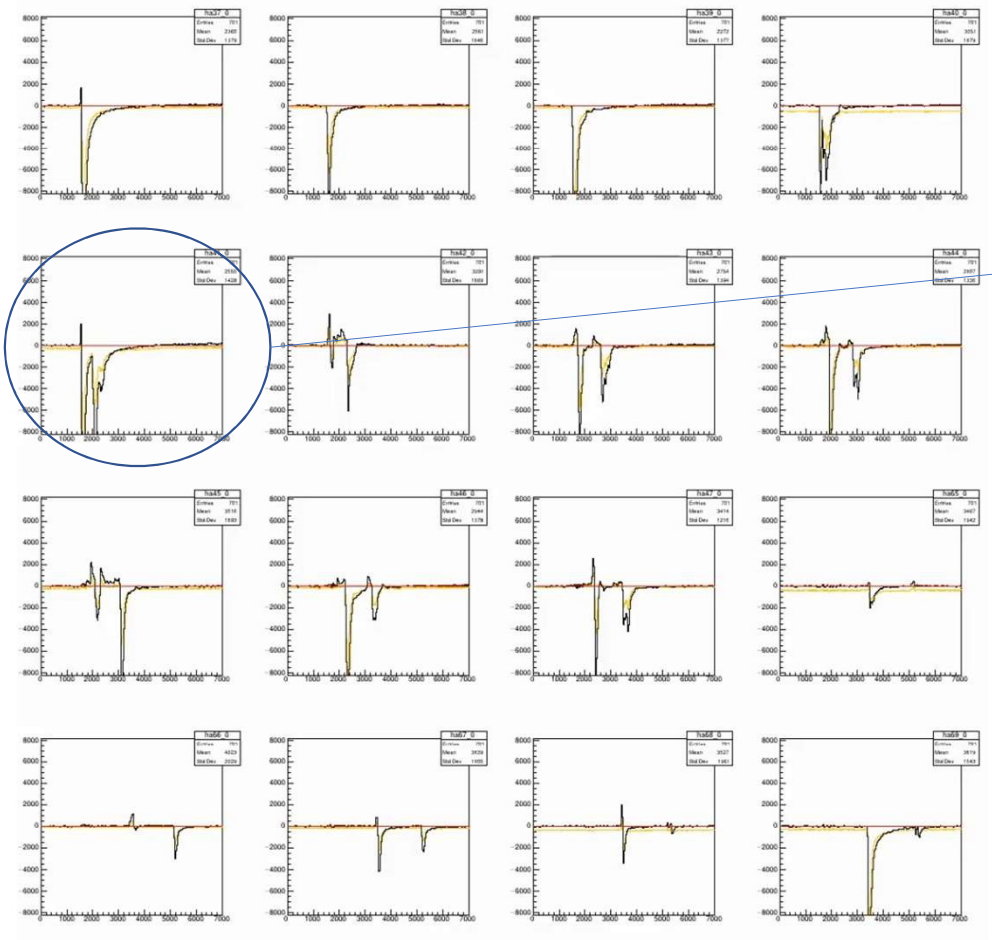


S1
S2
S1'
S2'
t0
S1'
S2'
S1'.S2' = t0
t1
t2
t3
t4
t5

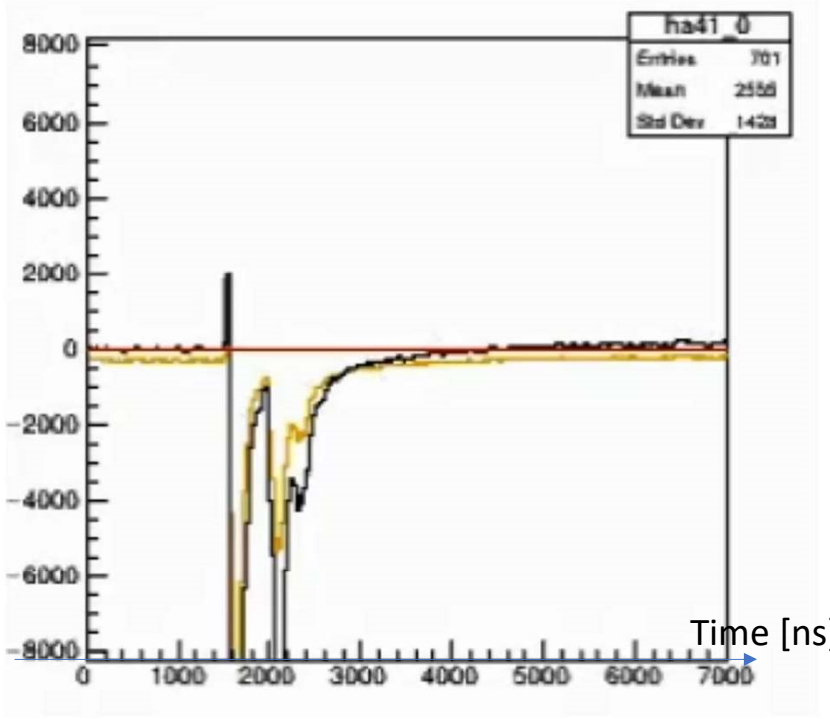

Detectors signals Wx


S1
PMT + Scintillating material
W4
W1
W3
W2
E
Gas volume
Detector type
Drift Chamber
t1
t2
t3
t4
t5
150
100
50
0
−50
−100
−150
−150 −100 −50 0 50 100 150
S2
PMT + Scintillating material

Data Analysis - Deconvolution



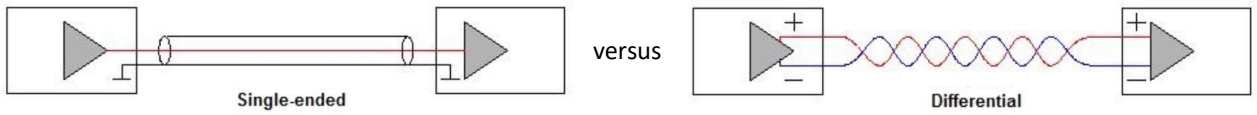
Yellow : Original signal
Red : Signal evolution during the deconvolution
Black : Residual signal

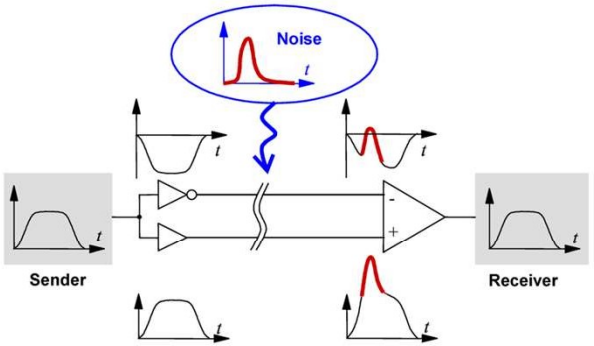


Have fun during the hands-on lab projects!

Things to consider

- Signal disturbance
  - Electromagnetic Interference (EMI) - surrounding equipment, power supply
  - Ground Loop - signal return path
  - Signal shielding - cable bundle extra shielding
  - Media transmission (electric cable coax, twisted pair, optical)
    - Transmission path - signal degradation
    - Attenuation - signal loss
    - Impedance - matching Z, termination resistor
    - Cross-talk - interference between neighbouring channels
- Signal type selection
  - Single-ended versus differential signals





Interesting links

https://www.analog.com/en/analog-dialogue/articles/understanding-and-eliminating-1-f-noise.html
https://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/dual-slope-type-adc/
https://www.electronicdesign.com/adc/what-s-difference-between-sar-and-delta-sigma-adcs
https://www.analog.com/en/design-center/interactive-design-tools/sigma-delta-adc-tutorial.html
Pipelined ADC: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023

https://midas.triumf.ca/MidasWiki/index.php/Main_Page

MWPC, TGC, RPC, DCs, Gas, µMega, GEM, Silicon detectors
https://indico.cern.ch/event/414089/attachments/844949/1175513/a02876s1t2.pdf